RELIABILITY REPORT

FOR

MAX6650EUB

PLASTIC ENCAPSULATED DEVICES

January 27, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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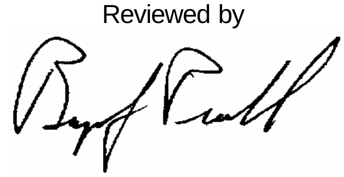
Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX6650 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6650 fan controller uses an SMBus™/I 2 C™-compatible interface to regulate and monitor the speed of 5VDC/12VDC brushless fans with built-in tachometers. It automatically forces the fan's tachometer frequency (fan speed) to match a preprogrammed value in the Fan-Speed Register by using an external MOSFET or bipolar transistor to linearly regulate the voltage across the fan.

The MAX6650 provides general-purpose input/output (GPIO) pins that serve as digital inputs, digital outputs, or various hardware interfaces. Capable of sinking 10mA, these open-drain inputs/outputs can drive an LED. To add additional hardware control, configure GPIO1 to fully turn on the fan in case of software failure. To generate an interrupt when a fault condition is detected, configure GPIO0 to behave as an active-low alert output.

The MAX6650 is available in a space-saving 10-pin µMAX package

B. Absolute Maximum Ratings

Item	Rating
V_{CC} to GND	-0.3V to +6V
FB, TACH_	-0.3V to +13.2V
All Other Pins	-0.3V to (V_{CC} + 0.3V)
Output Voltages	-0.3V to (V_{CC} + 0.3V)
Maximum Current	
Into V_{CC}, GND, V_{OUT}	100mA
Into All Other Pins	50mA
Continuous Power Dissipation (TA = +70°C)	
10-Pin µMAX	444mW
Derates above +70°C	
10-Pin µMAX	5.6mW/°C
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function: Fan-Speed Regulators and Monitors with SMBus/I 2 C-Compatible Interface

B. Process: TC06

C. Number of Device Transistors: 11,158

D. Fabrication Location: Taiwan

E. Assembly Location: Thailand, Philippines or Malaysia

F. Date of Initial Production: July, 2000

III. Packaging Information

A. Package Type: **10-Pin µMAX**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-1601-0097

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 60 x 86 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: Metal 1 - 0.9 microns / Metal 2 - 0.9 microns (as drawn)

F. Minimum Metal Spacing: Metal 1 - 0.9 microns / Metal 2 - 0.9 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

(4389:) Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.79 \times 10^{-9}$

λ = 6.79 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5530) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The MS34 die type has been found to have all pins able to withstand a transient pulse of ±600V Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA.

Table 1
Reliability Evaluation Test Results

MAX6650EEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	µMAX	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

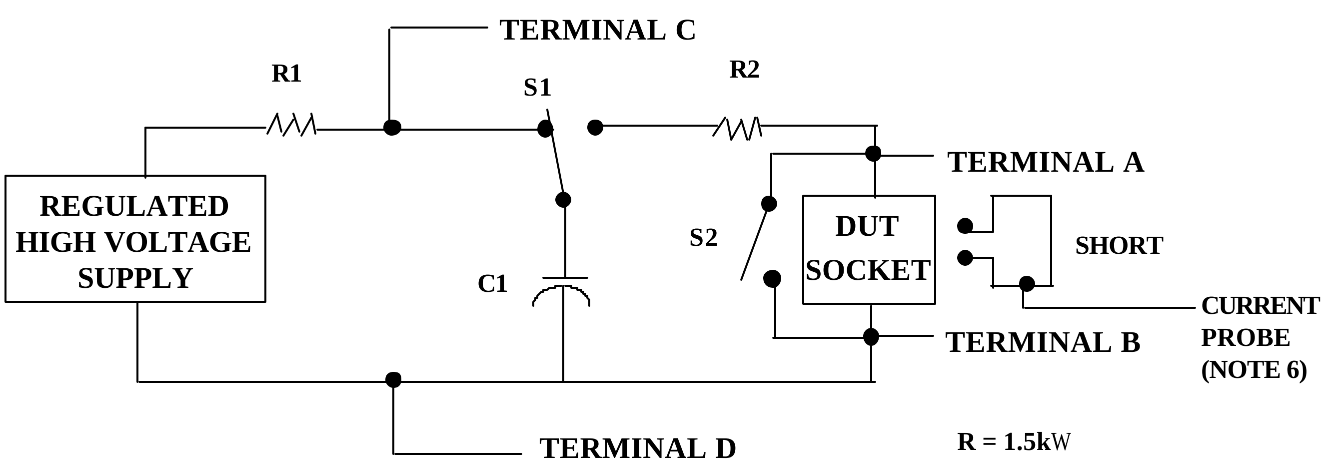
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S}$, $-V_{S}$, V_{REF}, etc).

3.4 Pin combinations to be tested.

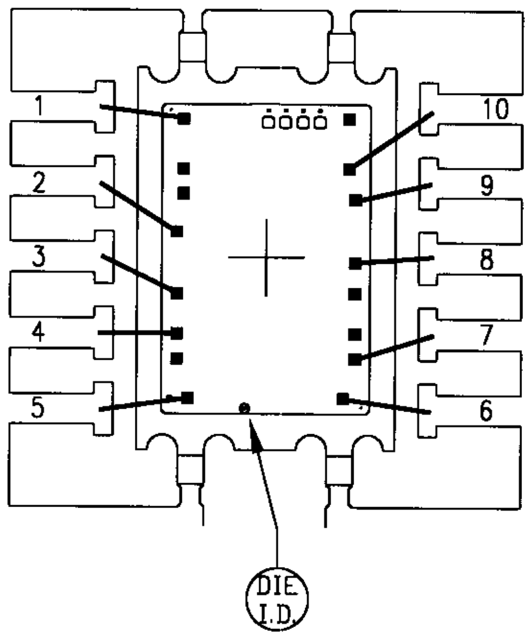
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



R = 1.5kW
C = 100pf

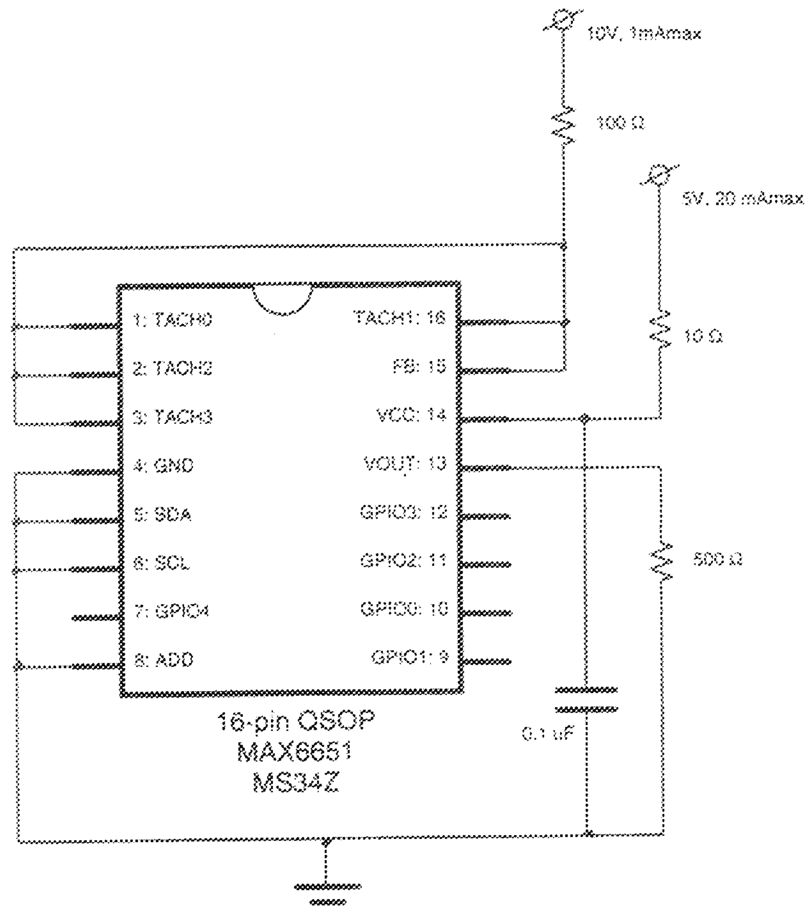


PKG.CODE: U10-2		APPROVALS	DATE
CAV./PAD SIZE: 68X94	PKG. DESIGN		

MAXIM

BUILDSHEET NUMBER:	REV.:
05-1601-0097	A

Burn-in Schematic MS34



06-5530