MAX6628MKA
Rev. A

RELIABILITY REPORT

FOR

MAX6628MKA

PLASTIC ENCAPSULATED DEVICES

September 30, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX6628 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6628 precise digital temperature sensor reports the temperature of a remote sensor. The remote sensor is a diode-connected transistor, typically a low-cost, easily mounted 2N3904 NPN type that replaces conventional thermistors or thermocouples. The MAX6628 can also measure the die temperature of other ICs, such as microprocessors (µPs) or microcontrollers (µCs) that contain an on-chip, diode-connected transistor.

Remote accuracy is ±1°C when the temperature of the remote diode is between 0°C and +125°C and the temperature of the MAX6628 is +30°C. The temperature is converted to a 12-bit + sign word with 0.0625°C resolution. The architecture of the device is capable of interpreting data as high as +145°C from the remote sensor. The MAX6628 temperature should never exceed +125°C.

This sensors is 3-wire serial interface SPI™ compatible, allowing the MAX6628 to be readily connected to a variety of µCs. The MAX6628 is a read-only device, simplifying it's use in systems where only temperature data is required.

Two conversion rates are available, one that continuously converts data every 0.5s (MAX6627), and one that converts data every 8s (MAX6628). The slower version provides minimal power consumption under all operating conditions (30µA, typ). Either device can be read at any time and provide the data from the last conversion.

The device operates with supply voltages between +3.0V and +5.5V, is specified between -55°C and +125°C, and come in the space-saving 8-pin SOT23 package.

B. Absolute Maximum Ratings

Item	Rating
All Voltages Referenced to GND	
VCC	-0.3V to +6V
SO, SCK, DXP, CS	-0.3V to VCC + 0.3V
DXN	-0.3V to +0.8V
SO Pin Current Range	-1mA to +50mA
Current Into All Other Pins	10mA
Operating Temperature Range	-55°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	Note 1
Continuous Power Dissipation (TA = +70°C)	
8-Pin SOT23	777mW
Derates above +70°C	
8-Pin SOT23	9.7mW/°C

Note 1: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the devicecan be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profilesrecommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and ConvectionReflow. Preheating is required. Hand or wave soldering is not allowed.

II. Manufacturing Information

A. Description/Function: Remote ±1°C Accurate Digital Temperature Sensors with SPI-Compatible Serial Interface

B. Process: S8 (Standard 0.8 micron silicon gate CMOS)

C. Number of Device Transistors: 6241

D. Fabrication Location: California, USA

E. Assembly Location: Malaysia

F. Date of Initial Production: July, 2001

III. Packaging Information

A. Package Type: **8-Pin SOT23 Flip-Chip**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: N/A

E. Bondwire: 8 mil dia. ball

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-2901-0009

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 45 x 90 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 0.8 microns (as drawn)

F. Minimum Metal Spacing: 0.8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.79 \times 10^{-9}$

λ = 6.79 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5658) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The TS05-1 die type has been found to have all pins able to withstand a transient pulse of ±1000V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA.

Table 1
Reliability Evaluation Test Results

MAX6628MKA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

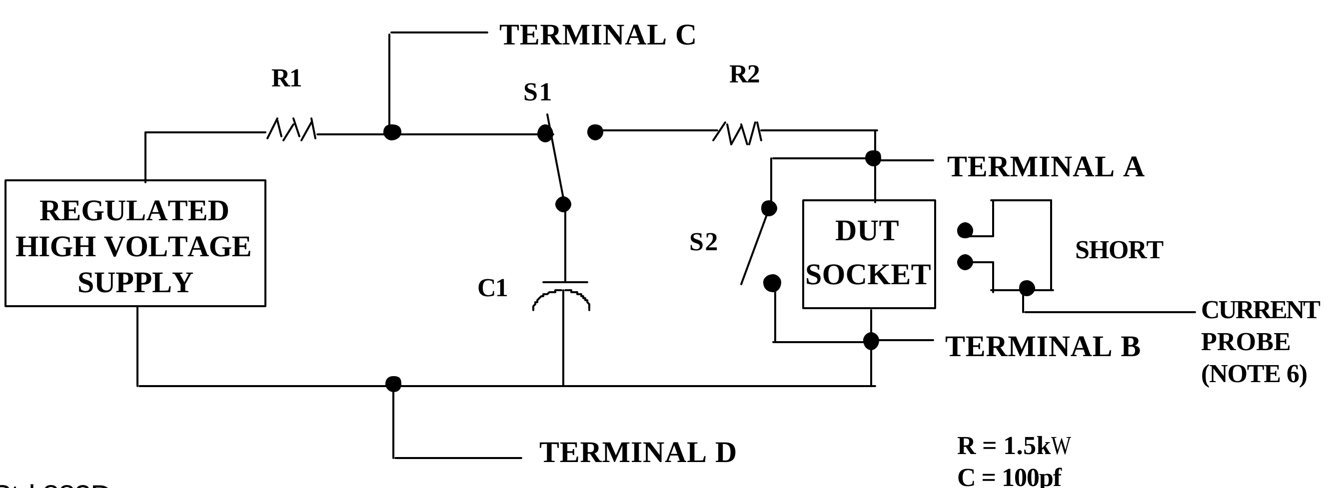
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

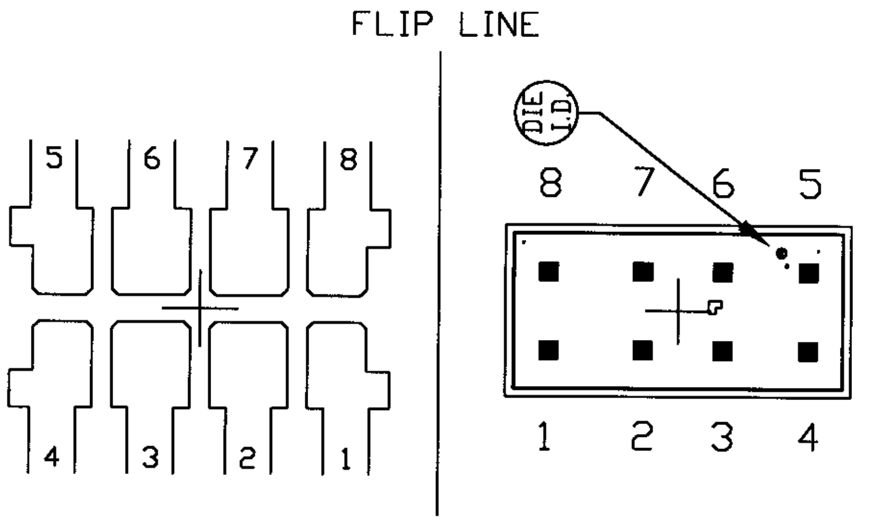
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



FLIP CHIP PKG.

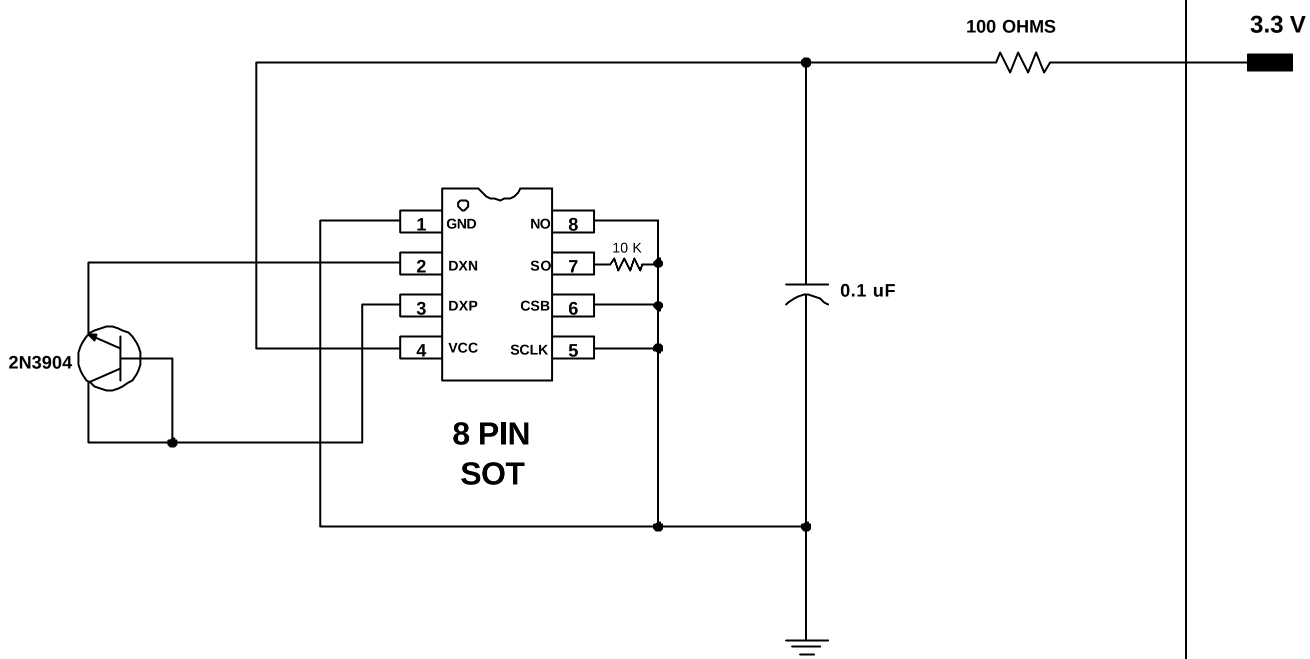


NOTE: CAVITY DOWN

PKG.CODE: K8F-4		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: FLIP CHIP	PKG. DESIGN			BUILDSHEET NUMBER: 05-2901-0009
				REV.: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES : MAX 6627, 6628

MAX. EXPECTED CURRENT = 1.5 mA

NOTES: