

RELIABILITY REPORT  
FOR  
**MAX6462xxxx**  
PLASTIC ENCAPSULATED DEVICES

February 2, 2004

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord  
Quality Assurance  
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl  
Quality Assurance  
Executive Director

## Conclusion

The MAX6462 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ....Device Description	V. ....Quality Assurance Information
II. ....Manufacturing Information	VI. ....Reliability Evaluation
III. ....Packaging Information	IV. ....Die Information
	.....Attachments

### I. Device Description

#### A. General

The MAX6462 Ultra-Low-Power Voltage Detector circuit monitors battery, power-supply, and system voltages. The circuit includes a precision bandgap reference, a comparator, internally trimmed resistor networks that set specified trip thresholds, and an internal 5% threshold hysteresis circuit (see the *Functional Diagram*). Output is asserted when  $V_{CC}$  falls below the internal  $V_{TH-}$  and remains asserted until  $V_{CC}$  rises above  $V_{TH+}$  ( $V_{TH+} = V_{TH-} \times 1.05$ ). This device provides excellent circuit reliability and low cost by eliminating external components and adjustments when monitoring nominal system voltages from +1.6V to +5.5V.

The MAX6462 is a voltage detectors with a propagation delay of 17 $\mu$ s.

The device is available with a push-pull with active-high output, three output stage. The device is available in SC70 and SOT23 packages specified over the -40°C to +125°C temperature range.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
(All voltages referenced to GND unless otherwise noted.)	
VCC	-0.3V to +7V
Push-Pull OUT/OUT	-0.3V to (VCC + 0.3V)
Input/Output Current (all pins)	20mA
Output Short Circuit (VCC or GND)	
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
3-Pin SC70	228.6mW
3-Pin SOT23	320mW
5-Pin SOT23	571mW
Derates above +70°C	
3-Pin SC70	2.9mW/°C
3-Pin SOT23	4.0mW/°C
5-Pin SOT23	7.1mW/°C

## II. Manufacturing Information

A. Description/Function:	Ultra-Low-Power Voltage Detectors
B. Process:	S8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors:	581
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	July, 2002

## III. Packaging Information

A. Package Type:	<b>3-Pin SOT23</b>	<b>3-Pin SC70</b>	<b>5-Pin SOT23</b>
B. Lead Frame:	Alloy 42	Copper or Alloy 42	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Non-Conductive Epoxy	Non-Conductive Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1601-0195	# 05-1601-0194	# 05-1601-0192
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1	Level 1

## IV. Die Information

A. Dimensions:	30 x 31 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information


- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Executive Director)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

 Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.57 \times 10^{-9}$$

$$\lambda = 13.57 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5681) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The MS81-1 die type has been found to have all pins able to withstand a transient pulse of  $\pm 1500\text{V}$  per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX6462xxxx**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23	77	0
			SC70	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

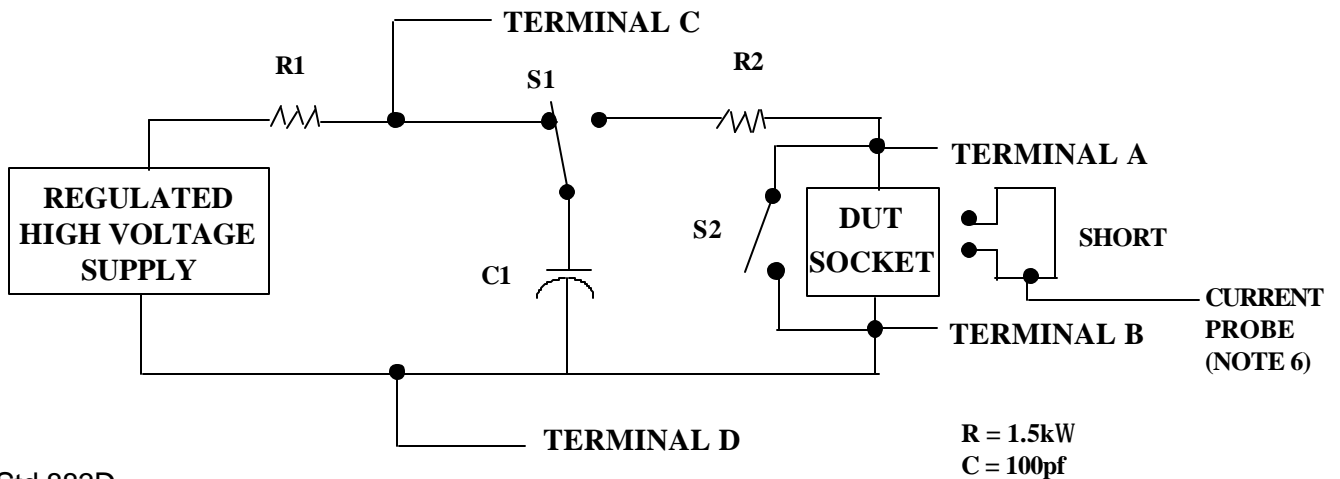
2/ No connects are not to be tested.

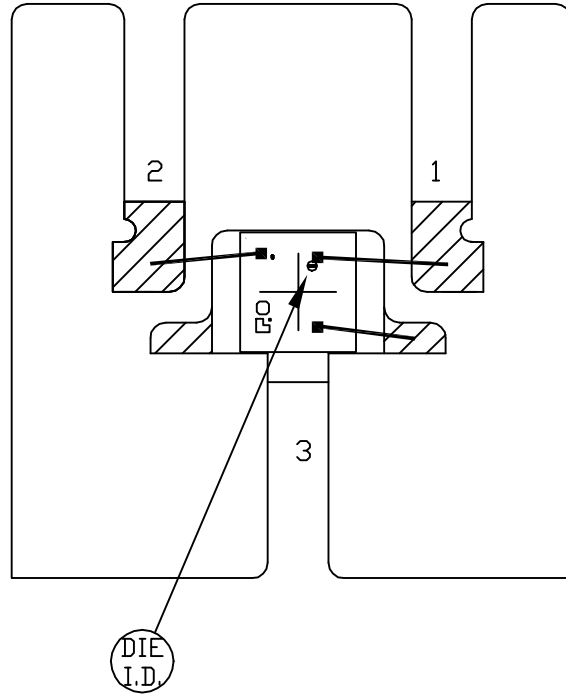
3/ Repeat pin combination 1 for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



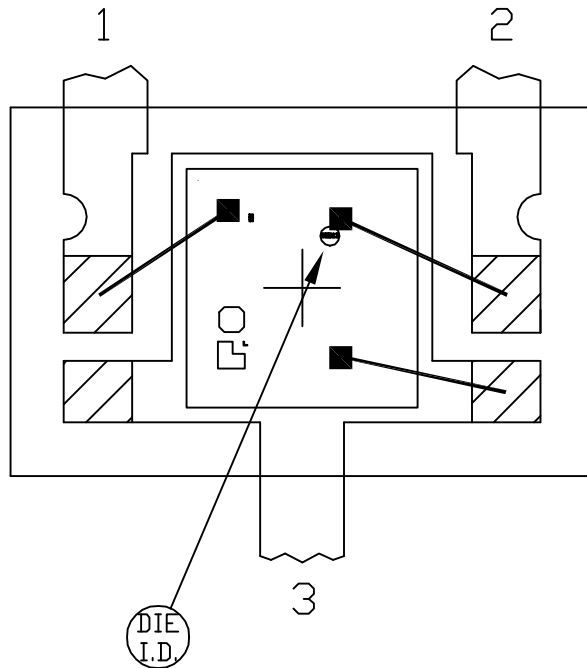


USE NON-CONDUCTIVE EPOXY



BONDING AREA

PKG. CODE: U3-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 45x32	PKG. DESIGN			BOND DIAGRAM #: 05-1601-0195	REV: A



USE NON-CONDUCTIVE EPOXY

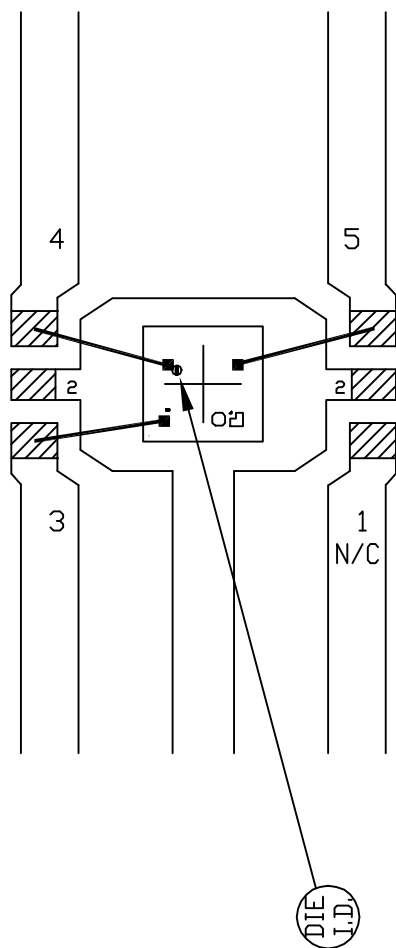
SCALE: 40x

CAVITY DOWN

 BONDABLE AREA

PKG. CODE: X3-2		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 34x35	PKG. DESIGN			BOND DIAGRAM #: 05-1601-0194	REV: A





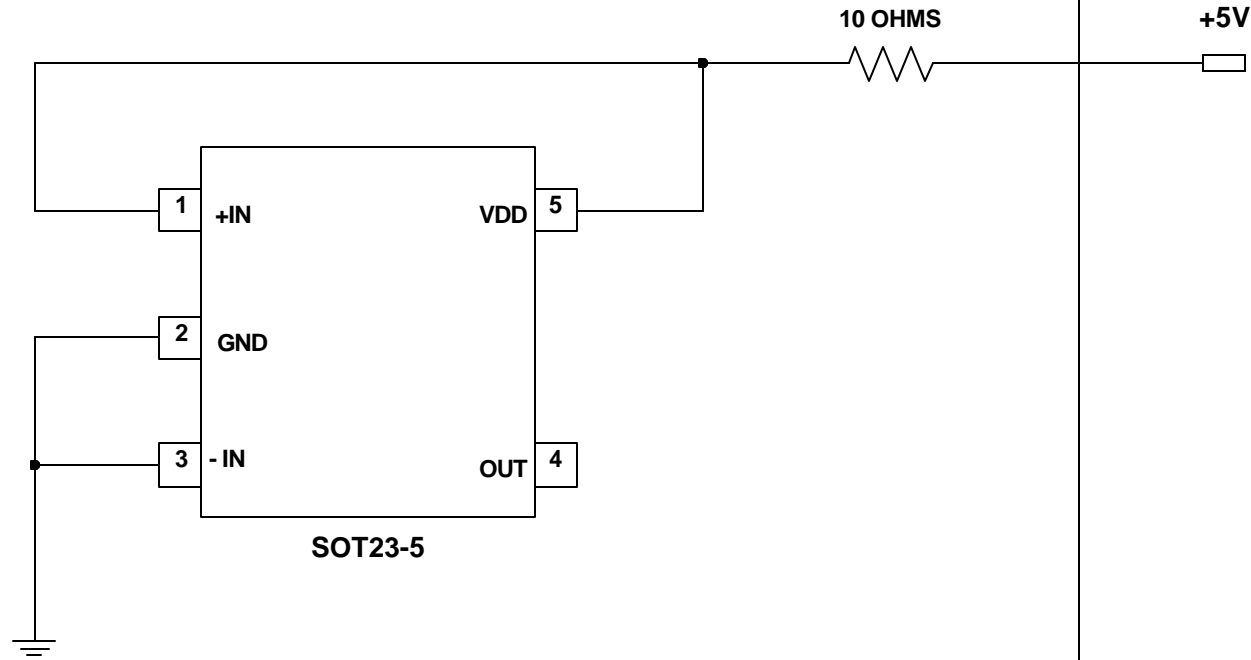
▨ - BONDING AREA

NOTE: CAVITY DOWN

PKG. CODE: U5-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 64X45	PKG. DESIGN			BOND DIAGRAM #: 05-1601-0192	REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 9021/ MAX 9031/6461/6841  
MAX. EXPECTED CURRENT = 5uA ( MAX 9021) 50uA ( MAX9031 )  
2.5uA (MAX6461) 40uA (MAX6841).

DRAWN BY: HAK TAN  
NOTES: