

RELIABILITY REPORT
FOR
MAX6425UK46+
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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Conclusion

The MAX6425UK46+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX6340/MAX6421/MAX6426 low-power microprocessor supervisor circuits monitor system voltages from 1.6V to 5V. These devices perform a single function: they assert a reset signal whenever the VCC supply voltage falls below its reset threshold. The reset output remains asserted for the reset timeout period after VCC rises above the reset threshold. The reset timeout is externally set by a capacitor to provide more flexibility. The MAX6421/MAX6424 have an active-low, push-pull reset output. The MAX6422 has an active-high, push-pull reset output and the MAX6340/MAX6423/MAX6425/MAX6426 have an active-low, open-drain reset output. The MAX6421/MAX6422/MAX6423 are offered in 4-pin SC70 or SOT143 packages. The MAX6340/MAX6424/MAX6425/MAX6426 are available in 5-pin SOT23-5 packages.

II. Manufacturing Information

A. Description/Function:	Low-Power, SC70/SOT μ P Reset Circuits with Capacitor-Adjustable Reset Timeout Delay
B. Process:	B8
C. Number of Device Transistors:	295
D. Fabrication Location:	California or Texas
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	AAA April 27, 2002

III. Packaging Information

A. Package Type:	5-pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Non-conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1601-0152
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	324.3 °C/W
K. Single Layer Theta Jc:	82 °C/W
L. Multi Layer Theta Ja:	255.9 °C/W
M. Multi Layer Theta Jc:	81 °C/W

IV. Die Information

A. Dimensions:	31X30 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 4340 \times 308 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 0.69 \times 10^{-9}$$

$$\lambda = 0.69 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.01 @ 25C and 0.26 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot J612EA005G, D/C 1028)

The MS70-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX6425UK46+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C	DC Parameters	70	0	I150BQ002B, D/C 0121
	Biased	& functionality	80	0	J612EA005I, D/C 1042
	Time = 1000 hrs.		78	0	J611EA017C, D/C 1201
			80	0	J610EA015G, D/C 1148

Note 1: Life Test Data may represent plastic DIP qualification lots.