

RELIABILITY REPORT
FOR
MAX6419UKxx
PLASTIC ENCAPSULATED DEVICES

May 2, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX6419 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX6419 low-power microprocessor supervisor circuit monitors system voltages from 1.6V to 5V. This device is designed to assert a reset signal whenever the V_{CC} supply voltage or RESET IN falls below its reset threshold or the manual reset input is asserted. The reset output remains asserted for the reset timeout period after V_{CC} and RESET IN rise above the reset threshold and the manual reset input is deasserted. The reset timeout is externally set by a capacitor to provide more flexibility.

The MAX6419 is offered with one fixed input and one adjustable input to monitor dual-voltage systems.

The MAX6419 has an active-high, push-pull reset. This device is offered in a SOT23-5 package and is fully specified from -40°C to +125°C.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Terminal Voltage (with respect to GND)	
V_{CC}	-0.3V to +6V
SRT, /MR, RESET IN	-0.3V to ($V_{CC} + 0.3V$)
RESET, /RESET (Push-Pull)	-0.3V to ($V_{CC} + 0.3V$)
Input Current (All Pins)	+/-20mA
Output Current (/RESET, RESET)	+/-20mA
Operating Temperature Range	-40°C to +85°C
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
5 Lead SOT-23	571mW
Derates above +70°C	
5 Lead SOT-23	7.1mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Power, Single/Dual-Voltage uP Reset Circuits
B. Process:	S8
C. Number of Device Transistors:	325
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	January, 2002

III. Packaging Information

A. Package Type:	5 Lead SOT-23
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0178
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	36 x 36 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Si
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

↓
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 24.13 \times 10^{-9} \quad \lambda = 24.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5889) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS60-7 die type has been found to have all pins able to withstand a transient pulse of $\pm 200\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 100\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX6419UKxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

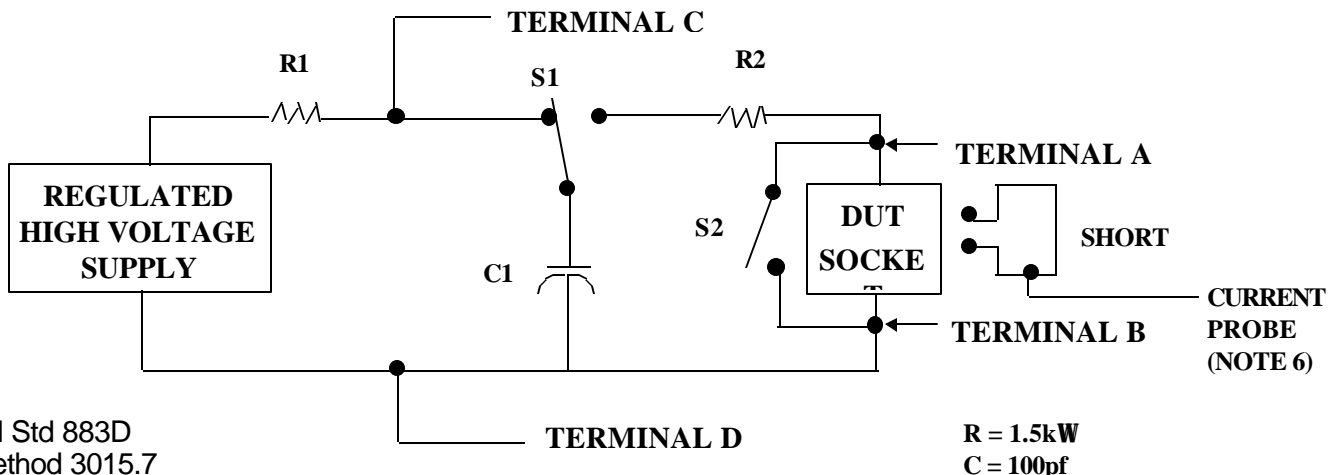
2/ No connects are not to be tested.

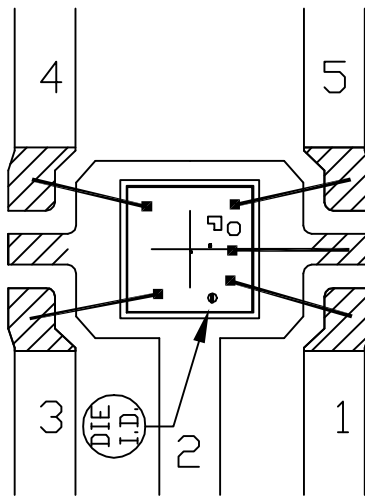
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



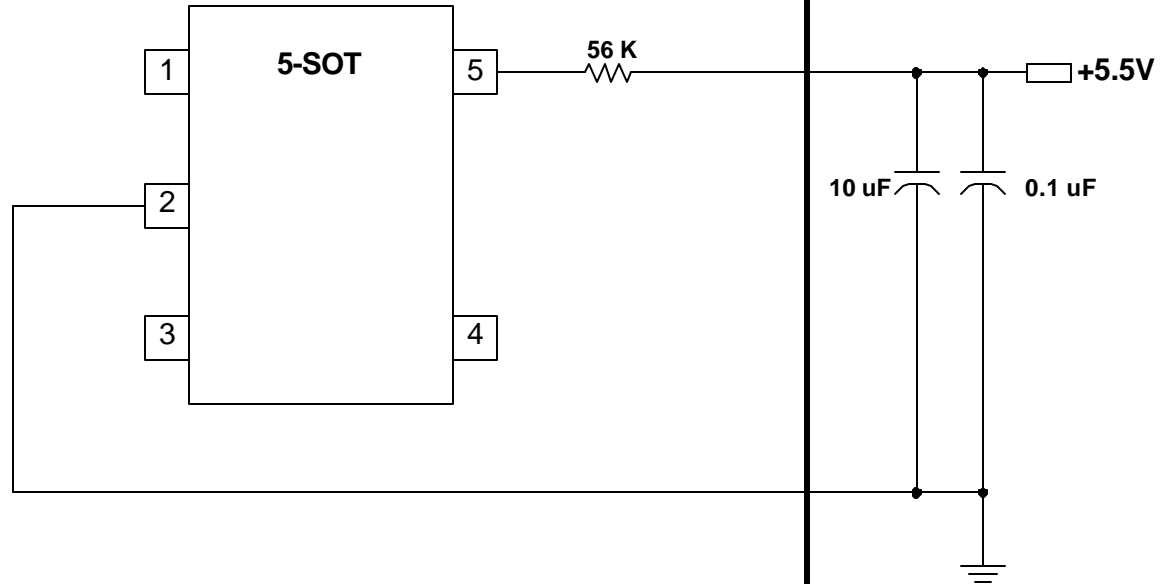


NOTE: CAVITY DOWN

PKG. CODE: U5-2		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 59x46	PKG. DESIGN			BOND DIAGRAM #: 05-1601-0178	REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 6412

DRAWN BY: HAK TAN

MAX. EXPECTED CURRENT = 100mA

NOTES: