

RELIABILITY REPORT
FOR
MAX5891EGK+
PLASTIC ENCAPSULATED DEVICES

February 18, 2010

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX5891EGK+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5891 advanced 16-bit, 600Msps, digital-to-analog converter (DAC) meets the demanding performance requirements of signal synthesis applications found in wireless base stations and other communications applications. Operating from 3.3V and 1.8V supplies, the MAX5891 DAC supports update rates of 600Msps using high-speed LVDS inputs while consuming only 298mW of power and offers exceptional dynamic performance such as 80dBc spurious-free dynamic range (SFDR) at $f_{OUT} = 30\text{MHz}$. The MAX5891 utilizes a current-steering architecture that supports a 2mA to 20mA full-scale output current range, and produces -2dBm to -22dBm full-scale output signal levels with a double-terminated 50 Ω load. The MAX5891 features an integrated 1.2V bandgap reference and control amplifier to ensure high-accuracy and low-noise performance. A separate reference input (REFIO) allows for the use of an external reference source for optimum flexibility and improved gain accuracy. The MAX5891 digital inputs accept LVDS voltage levels, and the flexible clock input can be driven differentially or single-ended, AC- or DC-coupled. The MAX5891 is available in a 68-pin QFN package with an exposed paddle (EP) and is specified for the extended (-40°C to +85°C) temperature range. Refer to the MAX5890 and MAX5889 data sheets for pin-compatible 14-bit and 12-bit versions of the MAX5891. [_____](#)

II. Manufacturing Information

A. Description/Function:	16-Bit, 600Msps, High-Dynamic-Performance DAC with LVDS Inputs
B. Process:	TS18
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Korea
F. Date of Initial Production:	January 20, 2005

III. Packaging Information

A. Package Type:	68-pin QFN 10x10
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1583
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	0.8°C/W
L. Multi Layer Theta Ja:	24°C/W
M. Multi Layer Theta Jc:	0.8°C/W

IV. Die Information

A. Dimensions:	153 X 143 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18μm
F. Minimum Metal Spacing:	0.18μm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.4 \times 10^{-9}$$
$$\lambda = 22.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The CD05-6 die type has been found to have all pins able to withstand a HBM transient pulse of +/-500 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX5891EGK+D

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data