

RELIABILITY REPORT
FOR
MAX5879EXF+
PLASTIC ENCAPSULATED DEVICES

September 16, 2011

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX5879EXF+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5879 is a high-performance, 14-bit, 2.3Gbps digital-to-analog converter (DAC) capable of synthesizing high-frequency and wideband signals in baseband and higher-order Nyquist zones. The 2.3Gbps update rate, combined with the selectable frequency-response modes (NRZ, RZ, RF, and RFZ), allows digital generation of signals to more than 2GHz output frequency. The unique RFZ mode allows generation up to the 6th Nyquist zone, with update rates to 1150Mbps. The device features excellent spurious, noise, and intermodulation distortion performance, and can directly synthesize signal bandwidths to more than 1GHz. The device has four 14-bit, multiplexed, low-voltage differential signaling (LVDS) input ports that each operates up to 1150Mbps. The DAC operates with a clock rate (fCLK) up to 2.3GHz. The device has a selectable 2:1 or 4:1 input multiplexer that allows the user to select two data ports up to 1150Mbps each, or four data ports up to 575Mbps each. In turn, the input data rate is 1/2 or 1/4 the DAC update rate at each port. The device features a delay-locked loop (DLL) to ease data synchronization with FPGAs or ASICs. The parity input and parity error flag output can be used to detect bit errors between the data source and the DAC. The device also features a data clock reset circuit for aligning the data-capture clocks of multiple DACs. The device has four selectable frequency-response output modes:

- Nonreturn-to-zero (NRZ) mode provides the highest dynamic range/output power in the 1st Nyquist zone.
- Return-to-zero (RZ) mode trades off SNR for improved gain flatness in the 1st, 2nd, and 3rd Nyquist zones.
- Radio-frequency (RF) mode provides higher SNR and excellent dynamic performance in the 2nd and 3rd Nyquist zones.
- Radio-frequency-return-to-zero (RFZ) mode provides high dynamic range and improved gain flatness in the 3rd through 6th Nyquist zones at a maximum update rate of fCLK/2. The device is a current-steering DAC with an integrated 50 differential output termination to ensure optimum dynamic performance. Operating from 3.3V and 1.8V power supplies, the device dissipates 1.8W at 40mA full-scale current and 2.3W at 80mA full-scale current. The device is specified over the -40°C to +85°C extended temperature range and is offered in a 256-ball (17mm x 17mm) CSBGA package.

II. Manufacturing Information

A. Description/Function:	14-Bit, 2.3Gbps Direct RF Synthesis DAC with Selectable Frequency Response
B. Process:	TS18
C. Number of Device Transistors:	326510
D. Fabrication Location:	Taiwan
E. Assembly Location:	Philippines
F. Date of Initial Production:	June 24, 2011

III. Packaging Information

A. Package Type:	CSBGA 17X17 256L
B. Lead Frame:	Copper
C. Lead Finish:	SnAgCu Balls, PdFree
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3681 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	3
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	25.9°C/W
M. Multi Layer Theta Jc:	5.6°C/W

IV. Die Information

A. Dimensions:	217.19 X 217.19 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18µm
F. Minimum Metal Spacing:	0.18µm
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25}^\circ\text{C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QP9ZBQ001D D/C 1120)

The CD15 die type has been found to have all pins able to withstand a HBM transient pulse of +/-500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX5879EXF+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	QP9ZBQ001D, D/C 1120

Note 1: Life Test Data may represent plastic DIP qualification lots.