RELIABILITY REPORT

FOR

MAX5805AAUB+

PLASTIC ENCAPSULATED DEVICES

September 13, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX5805AAUB+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5803/MAX5804/MAX5805 single-channel, low-power, 8-/10-/12-bit, voltage-output digital-to-analog converters (DACs) include output buffers and an internal reference that is selectable to be 2.048V, 2.500V, or 4.096V. The MAX5803/MAX5804/MAX5805 accept a wide supply voltage range of 2.7V to 5.5V with extremely low power (2C-compatible, 2-wire interface that operates at clock rates up to 400kHz. The DAC output is buffered and has a low supply current of 155µA (typical at 3V) and a low offset error of ±0.5mV (typical). On power-up, the MAX5803/MAX5804/MAX5805 reset the DAC outputs to zero, providing additional safety for applications that drive valves or other transducers which need to be off on power-up. The internal reference is initially powered down to allow use of an external reference. The MAX5803/MAX5804/MAX5805 include a user-configurable active-low asynchronous input, active-low AUX for additional flexibility. This input can be programmed to asynchronously clear (active-low CLR) or temporarily gate (active-low GATE) the DAC output to a user-programmable value. A dedicated active-low asynchronous LDAC input is also included. This allows simultaneous output updates of multiple devices. The MAX5803/MAX5804/MAX5805 are available in 10-pin TDFN/µMAX® packages and are specified over the -40°C to +125°C temperature range.

II. Manufacturing Information

A. Description/Function:	Ultra-Small, Single-Channel, 8-/10-/12-Bit Buffered Output Voltage DACs with Internal Reference and I²C Interface
B. Process:	S18
C. Number of Device Transistors:	22745
D. Fabrication Location:	California
E. Assembly Location:	Philippines or Thailand
F. Date of Initial Production:	November 30, 2012

III. Packaging Information

A. Package Type:	10-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4811
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	180°C/W K.
Single Layer Theta Jc:	41.9°C/W
L. Multi Layer Theta Ja:	113.1°C/W
M. Multi Layer Theta Jc:	41.9°C/W

IV. Die Information

A. Dimensions:	31.89X62.6 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 6.9 \times 10^{-9}$

$\lambda = 6.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot SAGG1Q001J, D/C 1218)

The DB50-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX5805AAUB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	80	0	SAGG1Q001M, D/C 1249
	Biased	& functionality	80	0	SAGG1Q001J, D/C 1218
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.