RELIABILITY REPORT

FOR

MAX5719GSD+T

PLASTIC ENCAPSULATED DEVICES

January 14, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX5719GSD+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5717 and MAX5719 are serial-input, unbuffered 16 and 20-bit voltage-output unipolar digital-to-analog converters (DACs) with integrated feedback resistors that allow bipolar operation when used with an external operational amplifier. These DACs provide low glitch energy, low noise, tight bipolar resistor matching, and high accuracy. The DACs feature ±4LSB INL (max, 16-bit) over the temperature range of -40°C to +105°C. Integrated precision setting resistors make the DACs easy to use. The MAX5717 and MAX5719 feature a 50MHz, 3-wire SPI(tm), QSPI(tm), MICROWIRE(tm), and DSP-compatible serial interface. On power-up, the output resets to zero-scale, providing additional safety for applications which drive valves or other transducers that need to be off on power-up. The DAC output settles in 750ns and has a low offset and gain drift of ±0.1 ppm/°C of FSR. The MAX5717 is functionally similar to the MAX542, but with significantly faster settling time. The MAX5719 provides a similar speed improvement as well as an increase in resolution to 20 bits.

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II. Manufacturing Information

A. Description/Function:	16- and 20-Bit Voltage DACs
B. Process:	S18
C. Number of Device Transistors:	125506
D. Fabrication Location:	USA
E. Assembly Location:	Philippines
F. Date of Initial Production:	June 24, 2016

III. Packaging Information

A. Package Type:	14-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Bondwire:	Au (1.3 mil dia.)
E. Mold Material:	Epoxy with silica filler
F. Assembly Diagram:	#05-9000-5620
G. Flammability Rating:	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
I. Single Layer Theta Ja:	120°C/W
J. Single Layer Theta Jc:	37°C/W
K. Multi Layer Theta Ja:	84°C/W
L. Multi Layer Theta Jc:	34°C/W

IV. Die Information

A. Dimensions:	75.9842X87.7953 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Brian Standley (Manager, Reliability)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The DB74-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX5719GSD+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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