RELIABILITY REPORT

FOR

MAX527DEWG+

PLASTIC ENCAPSULATED DEVICES

April 27, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX527DEWG+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX526/MAX527 contain four 12-bit, voltage-output digital-to-analog converters (DACs). Precision output buffer amplifiers are included on-chip to provide voltage outputs. The MAX527 operates with ±5V power supplies, while the MAX526 utilizes -5V and +12V to +15V supplies. Offset, gain, and linearity are factory calibrated to provide the MAX526â€™s 1LSB total unadjusted error (TUE). These devices feature double-buffered interface logic with a 12-bit input register and a 12-bit DAC register. Data in the DAC register sets the DAC output voltage. The MAX526/MAX527 have an 8-bit-wide data bus. Data is loaded into the input register using the two write operations with an 8-bit LSB write load and a 4-bit MSB write load. An asynchronous load DAC (active-low LDAC) input transfers data from the input register to the DAC register. All logic inputs are TTL and CMOS compatible. The MAX526/MAX527 are available in 24-pin, 300 mil plastic DIP, Ceramic SB, and wide SO packages.

II. Manufacturing Information

A. Description/Function:	Calibrated, Quad, Voltage-Output, 12-Bit DAC
B. Process:	SG5
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Philippines
F. Date of Initial Production:	April 22, 2000

III. Packaging Information

A. Package Type:	300 mil 24L SOIC
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0401-0388 / C
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	85°C/W
K. Single Layer Theta Jc:	18°C/W
L. Multi Layer Theta Ja:	60°C/W
M. Multi Layer Theta Jc:	20.5°C/W

IV. Die Information

A. Dimensions:	139 X 297 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 240 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 4.6 \times 10^{-9}$

$\lambda = 4.6$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the SG5 Process results in a FIT Rate of 0.12 @ 25C and 2.04 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NXEBCA005A D/C 9913)

The DA31-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-100mA.

Table 1
Reliability Evaluation Test Results

MAX527DEWG+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	80	0	NXEBCA005A, D/C 9937
	Biased	& functionality	80	0	XXEACA119C, D/C 9827
	Time = 192 hrs.		80	0	XXEBBA117D, D/C 9827

Note 1: Life Test Data may represent plastic DIP qualification lots.