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RELIABILITY REPORT

FOR

MAX5190BEEG+

PLASTIC ENCAPSULATED DEVICES

May 2, 2013

## MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

| Approved by |
| --- |
| Sokhom Chum |
| Quality Assurance |
| Reliability Engineer |

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**Conclusion**

The MAX5190BEEG+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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**I. Device Description**

A. General

The MAX5187 is an 8-bit, current-output digital-to-analog converter (DAC) designed for superior performance in signal reconstruction or arbitrary waveform generation applications requiring analog signal reconstruction with low distortion and low-power operation. The voltage-output MAX5190 provides equal specifications, with on-chip precision resistors for voltage output operation. Both devices are designed for a 10pV-s glitch operation to minimize unwanted spurious signal components at the output. An on-board +1.2V bandgap circuit provides a well-regulated, low-noise reference that can be disabled for external reference operation. The MAX5187/MAX5190 are designed to provide a high level of signal integrity for the least amount of power dissipation. They operate from a single supply of +2.7V to +3.3V. Additionally, these DACs have three modes of operation: normal, low-power standby, and full shutdown, which provides the lowest possible power dissipation with a 1µA (max) shutdown current. A fast wake-up time (0.5µs) from standby mode to full DAC operation allows for power conservation by activating the DAC only when required. The MAX5187/MAX5190 are packaged in a 24-pin QSOP and are specified for the extended (-40°C to +85°C) temperature range. For higher resolution, 10-bit versions, see the MAX5181/MAX5184 data sheet.

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## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 8-Bit, 40MHz, Current/Voltage-Output DACs |
| B. Process: | TS60 |
| C. Number of Device Transistors: | |
| D. Fabrication Location: | Taiwan |
| E. Assembly Location: | Malaysia, Philippines, Thailand |
| F. Date of Initial Production: | January 18, 2000 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 24-pin QSOP |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (1.3 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-0401-0506 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 105°C/W |
| K. Single Layer Theta Jc: | 34°C/W |
| L. Multi Layer Theta Ja: | 88°C/W |
| M. Multi Layer Theta Jc: | 34°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 85 X 97 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.6 microns (as drawn) |
| F. Minimum Metal Spacing: | 0.6 microns (as drawn) |
| G. Bondpad Dimensions: | |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

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**V. Quality Assurance Information**

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

**VI. Reliability Evaluation**

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 23.79 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 2504 \times 10^{-9}$

$\lambda$ = 2504 F.I.T. (60% confidence level @ 85°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS60 Process results in a FIT Rate of 1.14 @ 25C and 19.6 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (ESD lot K6BCBQ003D D/C 0320, Latch-Up lot K6BCBA054A D/C 1037)

The DA70-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-400V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

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**Table 1**
Reliability Evaluation Test Results

**MAX5190BEEG+**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | 80 | 0 | K6BCBQ002B, D/C 9947 |

Note 1: Life Test Data may represent plastic DIP qualification lots.

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