

RELIABILITY REPORT  
FOR  
MAX5144EUB+  
PLASTIC ENCAPSULATED DEVICES

December 8, 2013

**MAXIM INTEGRATED**

160 RIO ROBLES  
SAN JOSE, CA 95134

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## Conclusion

The MAX5144EUB+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX5141-MAX5144 are serial-input, voltage-output, 14-bit digital-to-analog converters (DACs) in tiny  $\mu$ MAX® packages, 50% smaller than comparable DACs in an 8-pin SO. They operate from low +3V (MAX5143/MAX5144) or +5V (MAX5141/MAX5142) single supplies. They provide 14-bit performance ( $\pm 1$  LSB INL and DNL) over temperature without any adjustments. The DAC output is unbuffered, resulting in a low supply current of 120 $\mu$ A and a low offset error of 2 LSBs. The DAC output range is 0V to VREF. For bipolar operation, matched scaling resistors are provided in the MAX5142/MAX5144 for use with an external precision op amp (such as the MAX400), generating a  $\pm$ VREF output swing. A 16-bit serial word is used to load data into the DAC latch. The 25MHz, 3-wire serial interface is compatible with SPI(tm)/QSPI(tm)/MICROWIRE(tm), and can interface directly with optocouplers for applications requiring isolation. A power-on reset circuit clears the DAC output to code 0 (MAX5141/MAX5143) or code 8192 (MAX5142/MAX5144) when power is initially applied. A logic low on active-low CLR asynchronously clears the DAC output to code 0 (MAX5141/MAX5143) or code 8192 (MAX5142/MAX5144), independent of the serial interface. The MAX5141/MAX5143 are available in 8-pin  $\mu$ MAX packages and the MAX5142/MAX5144 are available in 10-pin  $\mu$ MAX packages.

## II. Manufacturing Information

A. Description/Function:	+3V/+5V, Serial-Input, Voltage-Output, 14-Bit DACs
B. Process:	S6
C. Number of Device Transistors:	2778
D. Fabrication Location:	Japan
E. Assembly Location:	Philippines, Thailand, Malaysia
F. Date of Initial Production:	October 24, 2000

## III. Packaging Information

A. Package Type:	10-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0401-0537
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	180°C/W
K. Single Layer Theta Jc:	36°C/W
L. Multi Layer Theta Ja:	113.1°C/W
M. Multi Layer Theta Jc:	36°C/W

## IV. Die Information

A. Dimensions:	62 X 83 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.9 microns (as drawn)
F. Minimum Metal Spacing:	0.9 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- |                                   |   |
|-----------------------------------|---|
| A. Quality Assurance Contacts:    | Don Lipps (Manager, Reliability Engineering)<br>Bryan Preeshl (Vice President of QA)            |
| B. Outgoing Inspection Level:     | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% for all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm  |
| D. Sampling Plan:                 | Mil-Std-105D  |

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 79 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.9 \times 10^{-9}$$

$$\lambda = 13.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the C6Y Process results in a FIT Rate of 0.17 @ 25°C and 2.9 @ 55°C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot I22EQZ001G, D/C 0040)

The DA82 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

**Table 1**  
Reliability Evaluation Test Results

**MAX5144EUB+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	I22EQZ001G, D/C 0040

Note 1: Life Test Data may represent plastic DIP qualification lots.