

RELIABILITY REPORT  
FOR  
MAX513CSD+  
(MAX512, MAX513)  
PLASTIC ENCAPSULATED DEVICES

December 6, 2008

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
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## Conclusion

The MAX513CSD+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX512/MAX513 contain three 8-bit, voltage-output digital-to-analog converters (DAC A, DAC B, and DAC C). Output buffer amplifiers for DACs A and B provide voltage outputs while reducing external component count. The output buffer for DAC A can source or sink 5mA to within 0.5V of VDD or VSS. The buffer for DAC B can source or sink 0.5mA to within 0.5V of VDD or VSS. DAC C is unbuffered, providing a third voltage output with increased accuracy. The MAX512 operates with a single +5V  $\pm 10\%$  supply, and the MAX513 operates with a +2.7V to +3.6V supply. Both devices can also operate with split supplies. The 3-wire serial interface has a maximum operating frequency of 5MHz and is compatible with SPI<sup>®</sup>, QSPI<sup>®</sup>, and Microwire<sup>®</sup>. The serial input shift register is 16 bits long and consists of 8 bits of DAC input data and 8 bits for DAC selection and shutdown. DAC registers can be loaded independently or in parallel at the positive edge of CS. A latched logic output is also available for auxiliary control. Ultra-low power consumption and small packages (14-pin DIP/SO) make the MAX512/MAX513 ideal for portable and battery-powered applications. Supply current is only 1mA, dropping to less than 1 $\mu$ A in shutdown. Any of the three DACs can be independently shut down. In shutdown mode, the DAC's R-2R ladder network is disconnected from the reference input, minimizing system power consumption.

## II. Manufacturing Information

A. Description/Function:	Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface
B. Process:	S3
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Unisem Malaysia, ATP Philippines, UTL Thailand, Carsem Malaysia
F. Date of Initial Production:	Pre 1997

## III. Packaging Information

A. Package Type:	14-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0401-0419
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	120°C/W
K. Single Layer Theta Jc:	37°C/W

## IV. Die Information

A. Dimensions:	81 X 122 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)  
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 640 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 1.7 \times 10^{-9}$$

$\lambda = 1.7$  F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the S3 Process results in a FIT Rate of 1.7 @ 25C and 32.0 @ 55C (0.8 eV, 60% UCL)

### B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

### C. E.S.D. and Latch-Up Testing

The DA51 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX513CSD+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	640	0
<b>Moisture Testing</b> (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2) Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data