

RELIABILITY REPORT
FOR
MAX5106EEE
PLASTIC ENCAPSULATED DEVICES

March 30, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX5106 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	
IV.Die InformationAttachments

I. Device Description

A. General

The MAX5106 nonvolatile, quad, 8-bit digital-to-analog convertes (DAC) operates from a single +2.7V to +5.5V supply. An internal EEPROM stores the DAC states even after power is removed. Data from these nonvolatile registers automatically initialize the DAC outputs and operating states during power-up. Precision internal buffers swing Rail-to-Rail®, and the reference input range includes both ground and the positive rail.

The MAX5106 feature a software-controlled 10µA shutdown mode and a mute state that drives the DAC outputs to their respective REFL_ voltages.

The MAX5106 is available in a 16-pin QSOP package.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VDD, DIN, CS, CLK, MUTE to GND	-0.3V, +6V
DOUT, REFH_, REFL_, RDY/BSY, OUT_ to GND	-0.3V to (VDD + 0.3V)
Maximum Current into Any Pin	±50mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin QSOP	666.7mW
Derates above +70°C	
16-Pin PDIP	8.3mW/°C

II. Manufacturing Information

A. Description/Function:	Nonvolatile, Quad, 8-Bit DAC
B. Process:	TC05 (0.6 micron CMOS)
C. Number of Device Transistors:	32,000
D. Fabrication Location:	Taiwan, USA
E. Assembly Location:	Thailand or Philippines
F. Date of Initial Production:	July, 2001

III. Packaging Information

A. Package Type:	16-Pin QSOP
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-0401-0541
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020A:	Level 1

IV. Die Information

A. Dimensions:	84 x 128 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si/Cu (Aluminum/ Silicon/ Copper)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal 1: 0.6 microns; Metal 2: 0.7 microns (as drawn)
F. Minimum Metal Spacing:	Metal 1: 0.6 microns; Metal 2: 0.7 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Managing Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 13.57 \times 10^{-9} \quad \lambda = 13.57 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec #06-5568) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DA87Y die type has been found to have all pins able to withstand a transient pulse of $\pm 2000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX5106EEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

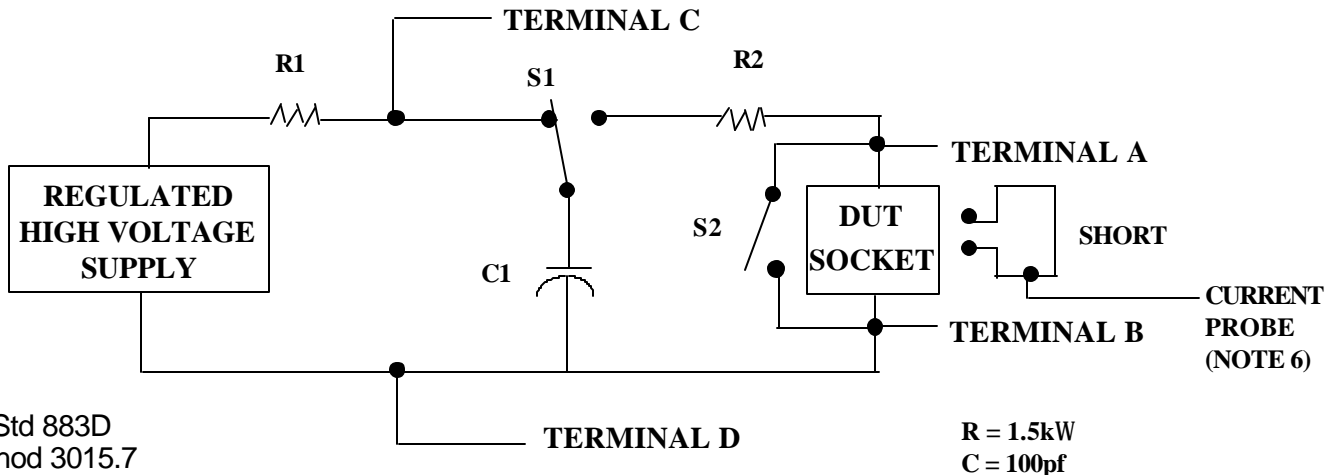
2/ No connects are not to be tested.

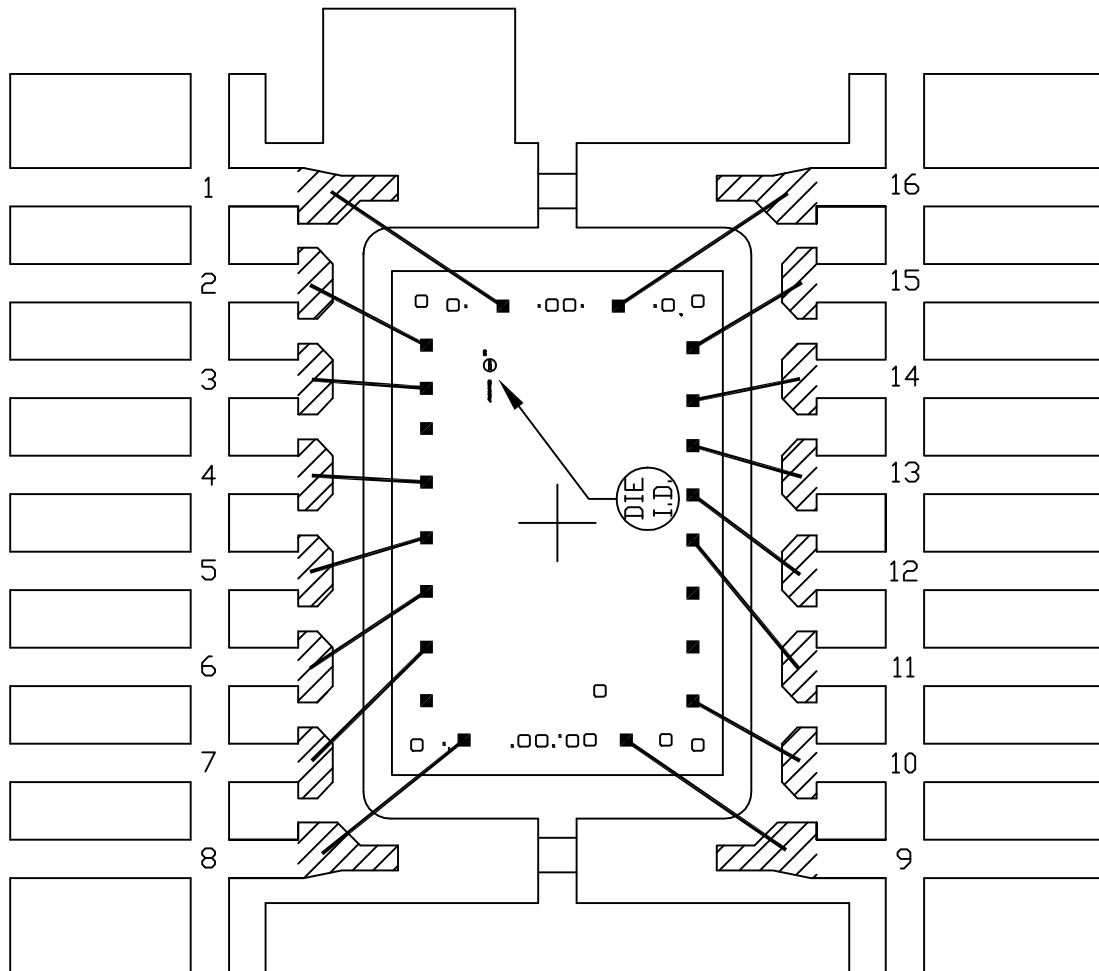
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

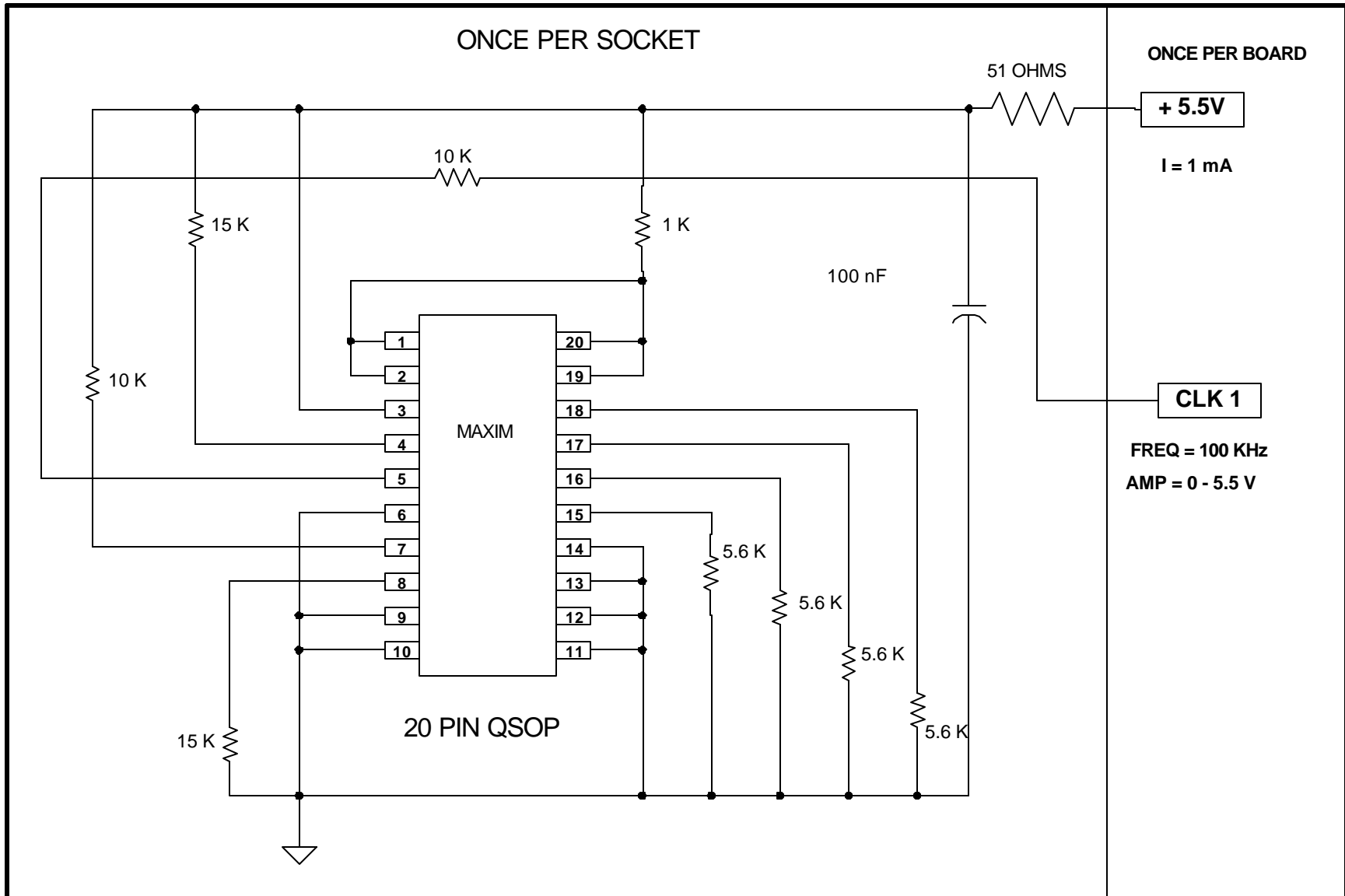
- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





 BONDABLE AREA

PKG. CODE: E16-5		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 101x154	PKG. DESIGN			BOND DIAGRAM #: 05-0401-0541	REV: B



DEVICES: MAX 5105

MAX. EXPECTED CURRENT = 1 mA