

RELIABILITY REPORT
FOR
MAX5040EUB
PLASTIC ENCAPSULATED DEVICES

July 13, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX5040 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	IV.Die Information
Attachments

I. Device Description

A. General

The MAX5040 provides intelligent control to power systems where two supply voltages need tracking. These cases include PowerPC®, DSP, and ASIC systems, which require a lower CORE voltage supply and a higher I/O voltage supply.

The MAX5040 controls the output voltage of the CORE and I/O supplies during power-up, power-down, and brownout situations. It ensures that the two power supplies rise or fall at the same rate, limiting the voltage difference between the CORE and I/O supplies. This eliminates stresses on the processor. The MAX5040 shuts down both the CORE and I/O supplies if either one is shorted or otherwise fails to come up.

The MAX5040 provides a power-OK (POK) signal that signals the processor if the CORE supply, the I/O supply, and the system bus supply (V_{CC}) are above their respective specified levels. The MAX5040 is targeted for nominal bus V_{CC} voltages from 4V to 5.5V. The MAX5040 works with CORE voltages ranging from 800mV to about 3V (depending on the gate-to-source turn-on threshold of the external N-channel MOSFET) and I/O voltages ranging from V_{CORE} to 4V. The MAX5040 provides tracking control of the I/O and CORE voltages using a single external N-channel MOSFET connected across it. This MOSFET is not in series with the power paths and does not dissipate any additional power during normal system operation. The external MOSFET is only on for brief periods during power-up/power-down cycling so a low-cost, small-size MOSFET with a rating of 1/4th to 1/8th of the normal supply current is suitable.

The MAX5040 is offered in space-saving 10-pin μ MAX packages.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
(All Voltages Referenced to GND)	
VCC, NDRV, SDO, and POK	-0.3V to +14V
CORE_FB, UVLO, I/O_SENSE, I/O, CORE	-0.3V to +4.25V
All Pins to VCC (except POK)	+0.3V
NDRV Continuous Current	50mA
Continuous Current, All Other Pins	20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
10-Pin μ MAX	444mW
Derates above +70°C	
10-Pin μ MAX	5.6mW/°C

II. Manufacturing Information

- A. Description/Function: Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs
- B. Process: BCD80
- C. Number of Device Transistors: 1272
- D. Fabrication Location: Oregon or California, USA
- E. Assembly Location: Thailand, Malaysia or Philippines
- F. Date of Initial Production: May, 2002

III. Packaging Information

- A. Package Type: **10-Pin μ MAX**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Silver-filled Epoxy
- E. Bondwire: Gold (1.3 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: # 05-1301-0050
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

- A. Dimensions: 52 X 64 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 3 microns (as drawn)
- F. Minimum Metal Spacing: 3 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information


- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

 Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 24.13 \times 10^{-9}$$

$$\lambda = 24.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5900) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The NP34-1 die type has been found to have all pins able to withstand a transient pulse of $\pm 1000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX5040EUB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

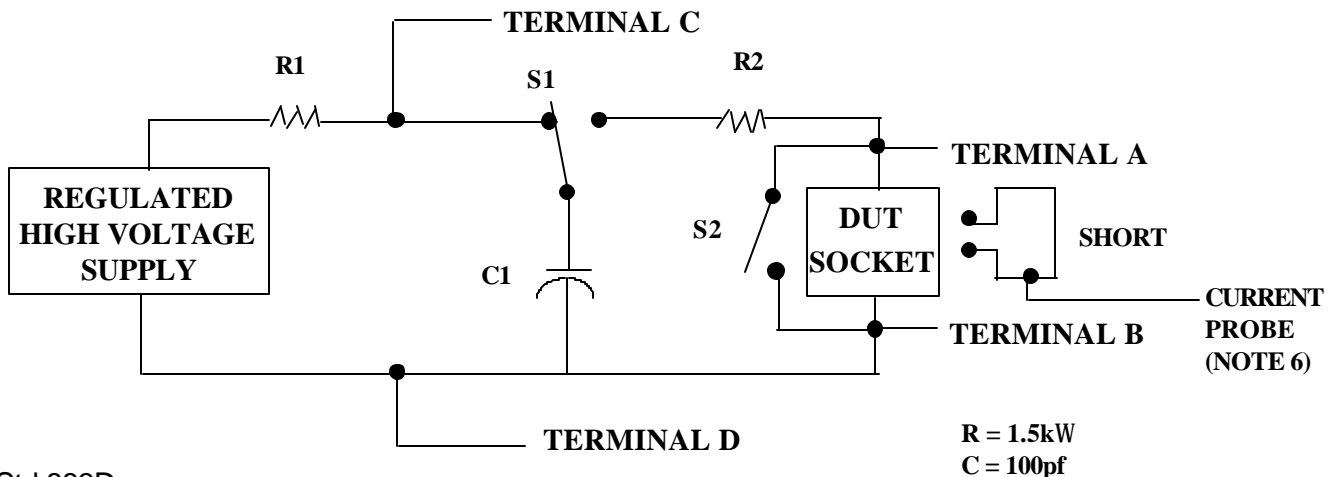
2/ No connects are not to be tested.

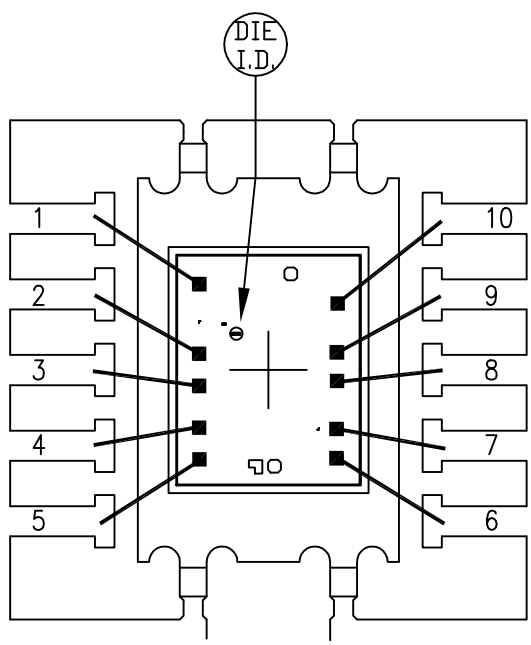
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: U10-2

SIGNATURES

DATE



CAV./PAD SIZE:
68x94

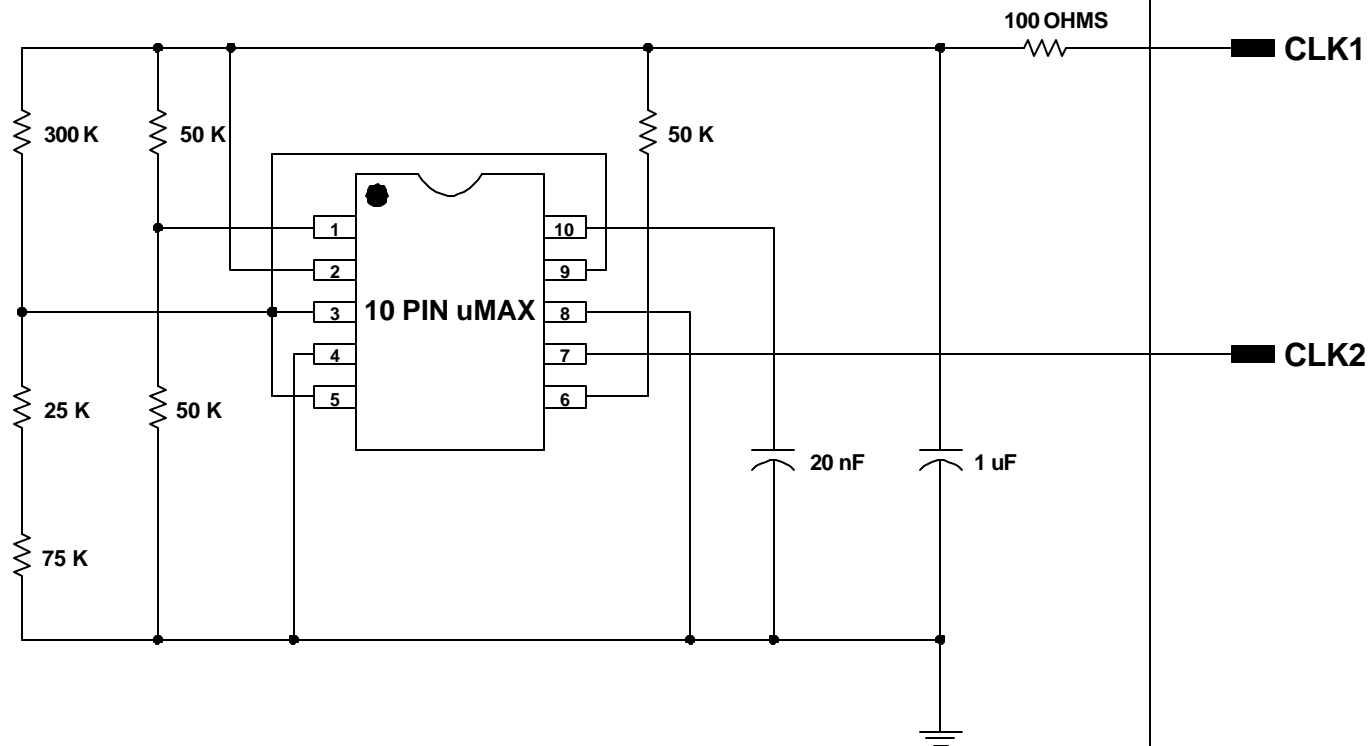
PKG.
DESIGN

BOND DIAGRAM #:
05-1301-0050

REV:
A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 5040

MAX. EXPECTED CURRENT = 4mA

DRAWN BY: TEK TAN

NOTES: CLK1 = 200 Hz (0V to 12V).
CLK2 = 8.3 KHz (0V to 2V).