RELIABILITY REPORT

FOR

MAX4996ETG+T

PLASTIC ENCAPSULATED DEVICES

June 14, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX4996ETG+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4996/MAX4996L triple DPDT analog switches operate from a single +2.5V to +5.5V supply, and feature 2.0 (typ) on resistance, low 6pF (typ) on-capacitance, and low power-supply current consumption. The MAX4996/MAX4996L combine the low capacitance and low resistance necessary for high-frequency switching applications in portable electronics. The MAX4996/MAX4996L have three logic inputs to control the switches in pairs. The MAX4996 has an active-high enable input (EN) to disable the switches, while the MAX4996L has an active-low enable input (active-low EN) to disable the switches. The enable input decreases the supply current and also places the COM_ outputs in a high-impedance state. The MAX4996/MAX4996L feature a 5µA (max) supply-current consumption when the logic inputs are not rail-to-rail. This feature is especially valuable in applications where direct interface to low-voltage processors is necessary. The MAX4996/MAX4996L are available in a space-saving 24-pin (3.5mm x 3.5mm) TQFN package and operate over the -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	Triple DPDT, Low-Capacitance Data Switches
B. Process:	S45
C. Number of Device Transistors:	1143
D. Fabrication Location:	Texas
E. Assembly Location:	Thailand
F. Date of Initial Production:	January 26, 2008

III. Packaging Information

A. Package Type:	24-pin TQFN 3.5x3.5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3015
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	65.1°C/W
K. Single Layer Theta Jc:	5°C/W
L. Multi Layer Theta Ja:	65.1°C/W
M. Multi Layer Theta Jc:	5.4°C/W

IV. Die Information

A. Dimensions:	41 X 45 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 96 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.5 \times 10^{-9}$

$\lambda = 11.5$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TKIYBQ00IC D/C 0815)

The AJ45-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX4996ETG+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	48	0	TKIZBQ001C, D/C 0815
	Biased	& functionality	48	0	TKIZA3001B, D/C 0742
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.