RELIABILITY REPORT

FOR

MAX4932EWC+T

WAFER LEVEL DEVICES

June 28, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineer

Conclusion

The MAX4932EWC+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4908/MAX4909/MAX4930/MAX4932 dual 3:1 clickless audio multiplexers feature negative-signal capability that allows signals as low as V CC - 5.5V to pass through without distortion. These analog multiplexers have a low on-resistance (0.38), low supply current, and operate from a single +1.8V to +5.5V supply.

The MAX4908 has shunt resistors on all input terminals, and the MAX4909 has shunt resistors on all input terminals except X0 and Y0. The MAX4930 has shunt resistors only on the X2 and Y2 terminals, and the MAX4932 has no shunt resistors. The shunt resistor feature reduces click-and-pop sounds by automatically discharging the capacitance at the input terminal when they are not connected. A break-before-make feature further reduces popping.

The MAX4908/MAX4909/MAX4930/MAX4932 use two digital control inputs CB1 and CB2 to switch between signals. The digital control inputs can accept up to +5.5V independent of the supply voltage.

The MAX4908/MAX4909/MAX4930/MAX4932 are available in 12-bump WLP and 14-pin TDFN-EP packages and operate over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	Dual 3:1 Clickless Audio Multiplexers with Negative-Signal Handling
B. Process:	S45
C. Number of Device Transistors:	1280
D. Fabrication Location:	USA
E. Assembly Location:	Japan
F. Date of Initial Production:	July 28, 2007

III. Packaging Information

A. Package Type:	12-bump WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-3014
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	62°C/W
M. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	80X61 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 47 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AS72-7 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX4932EWC+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	47	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.