



RELIABILITY REPORT
FOR
MAX4889BETO+T
PLASTIC ENCAPSULATED DEVICES

August 14, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
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Approved by
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Quality Assurance
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Conclusion

The MAX4889BETO+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4889B/MAX4889C high-speed passive switches route PCI Express® (PCIe) data between two possible destinations in desktop or notebook PCs. The MAX4889B/MAX4889C are quad double-pole/double-throw (4 x DPDT) switches ideal for switching four half lanes of PCIe data between two destinations. The MAX4889B/MAX4889C feature a single digital control input (SEL) to switch signal paths. The MAX4889C is intended for use in systems (e.g., SAS) where both the input and output are capacitively coupled, and provides a 10 μ A (typ) source current and a 60k (typ) internal biasing resistor to GND at the _OUT_ terminals. The MAX4889B/MAX4889C are fully specified to operate from a single +3.3V (typ) power supply. Both devices are available in an industry-standard 3.5mm x 9.0mm, 42-pin TQFN package. These devices operate over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	2.5/5.0/8.0Gbps PCIe Passive Switch
B. Process:	TS18
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Taiwan and Thailand
F. Date of Initial Production:	April 26, 2008

III. Packaging Information

A. Package Type:	42-pin TQFN 3.5x9
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#31-4852
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	39°C/W
K. Single Layer Theta Jc:	2°C/W
L. Multi Layer Theta Ja:	28°C/W
M. Multi Layer Theta Jc:	2°C/W

IV. Die Information

A. Dimensions:	54 X 94 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.23 / Metal 2-5 = 0.28 / Metal6 = 0.44 micron (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.23 / Metal2-4 = 0.28 / Metal5 = 0.46 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 96 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 11.5 \times 10^{-9}$$

$$\lambda = 11.5 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.15 @ 25C and 2.5 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AJ13 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114 (lot NDMTAAAB, D/C 0807)
ESD-CDM:	+/- 750V per JEDEC JESD22-C101 (lot NDMTAAK, D/C 0941)

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78 (lot NDMTAAAB, D/C 0807).

Table 1
Reliability Evaluation Test Results

MAX4889BETO+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135C	DC Parameters	48	0	NDMTAAB, D/C 0807
	Biased	& functionality	48	0	QOBYAQ002F, D/C 1030
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.