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RELIABILITY REPORT

FOR

MAX4865LELT+T

PLASTIC ENCAPSULATED DEVICES

January 13, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

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Conclusion

The MAX4865LELT+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. ....Device Description

II. ....Manufacturing Information

III. ....Packaging Information

.....Attachments

IV. ....Die Information

V. ....Quality Assurance Information

VI. ....Reliability Evaluation

I. Device Description

A. General

The MAX4864L/MAX4865L/MAX4866L/MAX4867 overvoltage protection controllers protect low-voltage systems against high-voltage faults up to +28V, and negative voltages down to -28V. These devices drive a low-cost complementary MOSFET. If the input voltage exceeds the overvoltage threshold, these devices turn off the n-channel MOSFET to prevent damage to the protected components. If the input voltage drops below ground, the devices turn off the p-channel MOSFET to prevent damage to the protected components. An internal charge pump eliminates the need for external capacitors and drives the MOSFET GATEN for a simple, robust solution. The overvoltage thresholds are preset to +7.4V (MAX4864L), +6.35V (MAX4865L), +5.8V (MAX4866L), and +4.65V (MAX4867). When the input voltage drops below the undervoltage lockout (UVLO) threshold, the devices enter a low-current standby mode (8.5µA). Also in shutdown (EN-bar set to logic-high), the current is reduced further (0.4µA). The MAX4864L/MAX4865L/MAX4866L have a +2.85V UVLO threshold, and the MAX4867 has a +2.5V UVLO threshold. In addition, a ±15kV ESD protection is provided to the input when bypassed with a 1µF capacitor to ground. All devices are offered in a small 6-pin SOT23 and a 6-pin, 2mm x 2mm µDFN package, and are specified for operation over the -40°C to +85°C temperature range.

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II. Manufacturing Information

A. Description/Function:	Overvoltage Protection Controllers with Reverse Polarity Protection
B. Process:	B8
C. Number of Device Transistors:	
D. Fabrication Location:	California or Texas
E. Assembly Location:	Thailand
F. Date of Initial Production:	January 22, 2005

III. Packaging Information

A. Package Type:	6-pin uDFN
B. Lead Frame:	Substrate
C. Lead Finish:	Gold
D. Die Attach:	Non-conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1648
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	223.6°C/W
M. Multi Layer Theta Jc:	122.1°C/W

IV. Die Information

A. Dimensions:	35X35 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 141 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.80 \times 10^{-9}$

λ = 7.80 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.01 @ 25C and 0.26 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TP1BBQ002C, 0523)

The AS51-5 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX4865LELT+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	96	0	TP1EBQ002B, D/C 0518
	Biased	& functionality	45	0	TP1GAQ001A, D/C 0449
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.

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