RELIABILITY REPORT

FOR

MAX4846ELT+T / MAX4846EYT+T

PLASTIC ENCAPSULATED DEVICES

February 20, 2014

**MAXIM INTEGRATED**

160 RIO ROBLES

SAN JOSE, CA 95134

| Approved by |
|---|
| Eric Wright |
| Quality Assurance |
| Reliability Engineering |

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**Conclusion**

The MAX4846ELT+T / MAX4846EYT+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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**I. Device Description**

A. General

The MAX4843-MAX4846 overvoltage protection controllers protect low-voltage systems against high-voltage faults of up to 28V. When the input voltage exceeds the overvoltage threshold, these devices turn off a low-cost, external n-channel FET(s) to prevent damage to the protected components. An internal charge pump eliminates the need for external capacitors and drives the FET gate for a simple, robust solution. The overvoltage trip level is set to 7.4V (MAX4843), 6.35V (MAX4844), 5.8V (MAX4845), or 4.65V (MAX4846). When the input voltage drops below the undervoltage lockout (UVLO) threshold, the devices enter a low standby current mode (10µA). The MAX4843/MAX4844/MAX4845 have a UVLO threshold of 4.15V, the MAX4845C/MAX4845D have a UVLO threshold of 2.2V, and the MAX4846 has a UVLO threshold of 2.5V. In addition to the single FET configuration, the devices can be configured with back-to-back external FETs to prevent currents from being back-driven into the adapter. An additional feature includes a ±15kV ESD-protected input when bypassed with a 1µF capacitor to ground. All devices are offered in small 6-pin µDFN (1.5mm x 1.0mm) and 6-pin ultra-thin LGA (MAX4845EYT+T only) (1.5mm x 1.0mm) packages and are specified for operation over the -40°C to +85°C temperature range.

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## II. Manufacturing Information

| | | |
|---|---|---|
| A. Description/Function: | Overvoltage Protection Controllers with Low Standby Current | |
| B. Process: | B8 | |
| C. Number of Device Transistors: | 102138 | |
| D. Fabrication Location: | USA | |
| E. Assembly Location: | Taiwan, Thailand | Taiwan, Thailand |
| F. Date of Initial Production: | April 20, 2005 | |

## III. Packaging Information

| | | |
|---|---|---|
| A. Package Type: | 6-pin uDFN | 6-bump UltraThin LGA |
| B. Lead Frame: | Substrate | Substrate |
| C. Lead Finish: | Gold | N/A |
| D. Die Attach: | Non-conductive | Non-conductive |
| E. Bondwire: | Au (1 mil dia.) | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-1770 | #05-9000-2796 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 | Level 1 |
| J. Single Layer Theta Ja: | N/A°C/W | N/A°C/W |
| K. Single Layer Theta Jc: | N/A°C/W | N/A°C/W |
| L. Multi Layer Theta Ja: | 477°C/W | 470°C/W |
| M. Multi Layer Theta Jc: | 122°C/W | 120°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 31 X 30 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/0.5%Cu with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 1.2 microns (as drawn) |
| F. Minimum Metal Spacing: | 0.8 microns (as drawn) |
| G. Bondpad Dimensions: | |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

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**V. Quality Assurance Information**

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

**VI. Reliability Evaluation**

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 46 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 23.9 \times 10^{-9}$

$\lambda$ = 23.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.05 @ 25°C and 0.9 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TYW3AQ001C, D/C 0507)

The AS52-3 die type has been found to have all pins able to withstand a HBM transient pulse of +/-600V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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**Table 1**
Reliability Evaluation Test Results

**MAX4846ELT+T / MAX4846EYT+T**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | 46 | 0 | TYW3AQ001C, D/C 0507 |

Note 1: Life Test Data may represent plastic DIP qualification lots.

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