

RELIABILITY REPORT
FOR
MAX4838EXT+
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

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Conclusion

The MAX4838EXT+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX4838-MAX4842 are overvoltage protection ICs that protect low-voltage systems against voltages of up to 28V. If the input voltage exceeds the overvoltage trip level, the MAX4838-MAX4842 turn off the low-cost external n-channel FET(s) to prevent damage to the protected components. An internal charge pump eliminates the need for external capacitors and drives the FET gate for a simple, robust solution. The MAX4838/MAX4839 have a 7.4V overvoltage threshold, and the MAX4840/MAX4841 have a 5.8V overvoltage threshold. The MAX4842 has a 4.7V overvoltage threshold. The MAX4838-MAX4841 have an undervoltage lockout (UVLO) threshold of 3.25V while the MAX4842 has a UVLO of 3.0V. In addition to the single FET configuration, the devices can be configured with back-to-back external FETs to prevent currents from being back-driven into the adapter. On power-up, the device waits for 50ms before driving GATE high. Active-low FLAG is held low for an additional 50ms after GATE goes high before deasserting. The MAX4838/MAX4840/MAX4842 have an open-drain active-low FLAG output, and the MAX4839/MAX4841 have a pushpull FLAG output. The active-low FLAG output asserts immediately to an overvoltage fault. Additional features include a 15kV ESD-protected input (when bypassed with a 1 μ F capacitor) and a shutdown pin (active-low EN) to turn off the device (MAX4838/MAX4840/MAX4842). All devices are offered in a small 6-pin SC70 package and are specified for operation from -40°C to +85°C.

II. Manufacturing Information

A. Description/Function:	Overvoltage Protection Controllers with Status FLAG
B. Process:	B8
C. Number of Device Transistors:	
D. Fabrication Location:	California or Texas
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	October 25, 2003

III. Packaging Information

A. Package Type:	6-pin SC70
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Non-conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0874
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	326°C/W
K. Single Layer Theta Jc:	115°C/W
L. Multi Layer Theta Ja:	326.5°C/W
M. Multi Layer Theta Jc:	115°C/W

IV. Die Information

A. Dimensions:	32 X 31 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 160 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 6.9 \times 10^{-9}$$

$$\lambda = 6.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.04 @ 25C and 0.73 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot SOG0AQ001C, D/C 0338)

The AS30 die type has been found to have all pins able to withstand a HBM transient pulse of +/-200V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX4838EXT+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C	DC Parameters	80	0	SOG0BQ002A, D/C 0409
	Biased	& functionality	80	0	SOG0AQ001C, D/C 0338
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.