

RELIABILITY REPORT
FOR
MAX4837ExTxx
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX4837 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4837 low-dropout linear regulator (LDOs) features an accurate current-limiting switch with an integrated FLAG-bar or RESET-bar function. This device operates from 2.5V to 5.5V and deliver up to 500mA of load current at a preset output voltage. Preset output voltage levels are 1.8V/2.5V/2.8V/3.0V/3.3V.

The MAX4837 offers a programmable softstart control function to eliminate false reset during startup. The MAX4837 provides a RESET-bar function to notify the system when the output drops below the threshold. Additionally, reverse-current protection prevents current flowing from the output to the input. Other features include a low 90 μ A quiescent current, a 0.1 μ A shutdown current.

The MAX4837 is available in space-saving 6-pin SOT23 and TDFN packages. Each device is specified over the -40°C to +85°C extended temperature range. Contact factory for other programmed output voltage versions from 1.5V to 3.3V in 100mV increments.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN, SHDN, FLAG, OUT to GND	-0.3V to +6V
RESET to GND	-0.3V to (VOUT + 0.3V)
SS to GND	-0.3V to (VIN + 0.3V)
IN to OUT	\pm 6V
OUT Short Circuit to GND	Continuous
All Pins ESD Handling (Human Body Model)	2kV
Continuous Power Dissipation (TA = +70°C)	
6-Pin SOT23 (derate 9.1mW/°C above +70°C)	727mW
6-Pin TDFN (derate 24.4mW/°C above +70°C)	1951.2mW
Operating Temperature Range	-40°C to +85°C
Operating Junction Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	500mA LDO Linear Regulators with Current-Limiting Switch
B. Process:	B8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors:	1,575
D. Fabrication Location:	California or Texas, USA
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	July, 2004

III. Packaging Information

A. Package Type:	6-Pin TDFN	6-Pin SOT23
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy	Non-Conductive Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	n/a
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0571	# 05-9000-0972
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions:	90 X 45 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 43 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

△ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 25.54 \times 10^{-9}$$

$$\lambda = 25.54 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-6294) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.17 @ 25°C and 2.92 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AS24-8 die type has been found to have all pins able to withstand a transient pulse of $\pm 600\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX4837ExTxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		43	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TDFN	77	0
			SOT	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

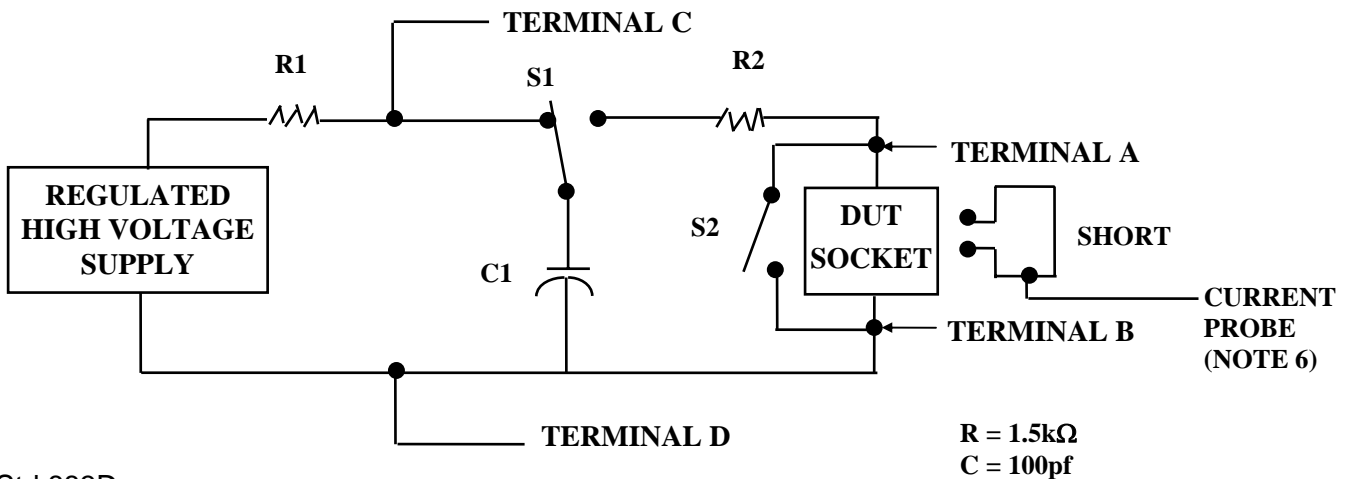
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

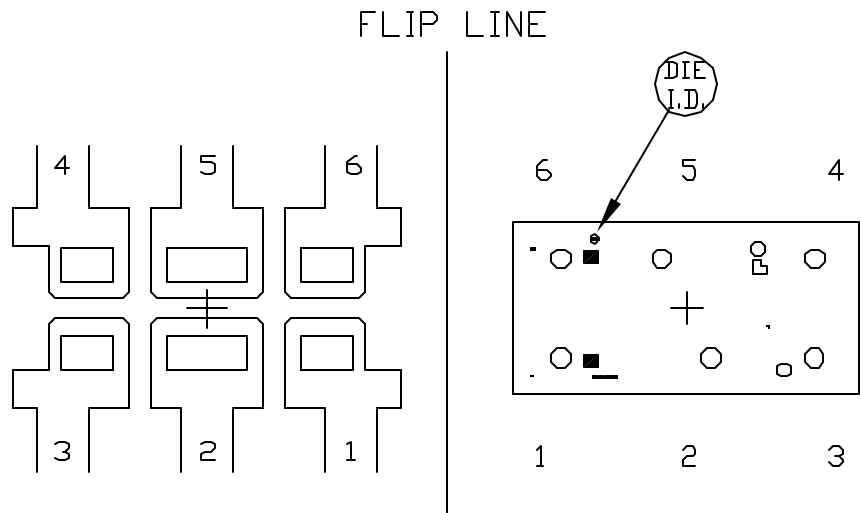
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



FLIP CHIP PKG.

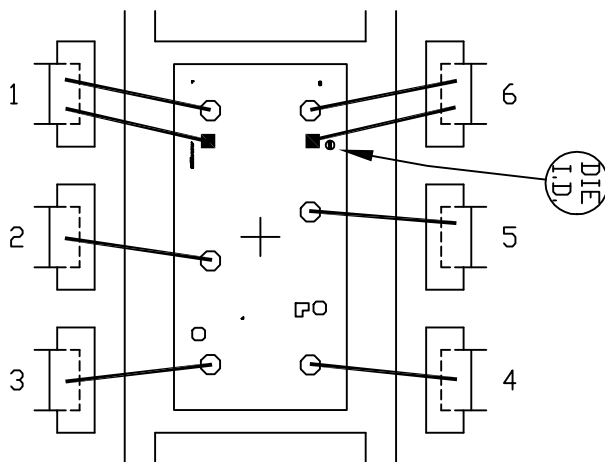


NOTE: CAVITY DOWN

PKG. CODE: U6F-6		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: FLIP CHIP	PKG. DESIGN			BOND DIAGRAM #: 05-9000-0972	REV: B

3x3x0.8 MM TDFN PKG.

EXPOSED PAD PKG.



PKG. CODE: T633-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 71x102	PKG. DESIGN			BOND DIAGRAM #: 05-9000-0971	REV: A

