RELIABILITY REPORT

FOR

MAX4784EUE+

PLASTIC ENCAPSULATED DEVICES

April 26, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

Conclusion

The MAX4784EUE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX4780/MAX4784 are low on-resistance, low-voltage, quad 2:1 analog multiplexers that operate from a single +1.6V to +4.2V supply. These devices have fast switching speeds (tON = 20ns, tOFF = 8ns), handle rail-to-rail analog signals, and consume less than 1µW of quiescent power. When powered from a +2.7V supply, the MAX4780/MAX4784 feature low 0.7 on-resistance (RON), and 0.1 RON flatness. The digital logic input is +1.8V CMOS-logic compatible when using a single +3V supply. The MAX4780/MAX4784 are available in 16-pin TSSOP and 3mm x 3mm thin QFN packages.

II. Manufacturing Information

A. Description/Function:	0.7 Ohm, Low-Voltage, Quad 2:1 Analog Multiplexers
B. Process:	TS35
C. Number of Device Transistors:	202
D. Fabrication Location:	Taiwan
E. Assembly Location:	Philippines or Malaysia
F. Date of Initial Production:	April 27, 2002

III. Packaging Information

A. Package Type:	16-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1201-0281
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	106°C/W
K. Single Layer Theta Jc:	27°C/W
L. Multi Layer Theta Ja:	90°C/W
M. Multi Layer Theta Jc:	27°C/W

IV. Die Information

A. Dimensions:	53 X 53 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35um
F. Minimum Metal Spacing:	0.35um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 44 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 4.8 \times 10^{-9}$

λ = 4.8 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.8 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot QD30BQ001C, D/C 0924)

The AH86 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX4784EUE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	44	0	QD30AQ001B, D/C 0203

Note 1: Life Test Data may represent plastic DIP qualification lots.