RELIABILITY REPORT

FOR

MAX4761ETX+T / MAX4761EWX+T

PLASTIC ENCAPSULATED DEVICES

November 17, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX4761ETX+T / MAX4761EWX+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX4760/MAX4760A/MAX4761/MAX4761A (DPDT) analog switches operate from a single +1.8V to +5.5V supply. These switches feature a low 54pF (typ) capacitance for high-speed data switching applications. The MAX4760/MAX4760A are a quad double-pole/double-throw (DPDT) switches and the MAX4761/MAX4761A are octal single-pole/double-throw (SPDT) switches. They have eight 2.0 Ω (typ) on-resistance, low-capacitance switches to route audio and data signals. The MAX4760/MAX4760A have 4 logic inputs to control the switches in pairs. The MAX4761/MAX4761A have one logic control input and an enable input (EN) to disable the switches. The MAX4760/MAX4760A/MAX4761/MAX4761A are available in a small 36-pin (6mm x 6mm) TQFN and 36-bump (3mm x 3mm) WLP package.

II. Manufacturing Information

A. Description/Function:	High-Bandwidth, Quad DPDT Switches
B. Process:	E35
C. Fabrication Location:	USA
D. Assembly Location:	Taiwan, China, Thailand
E. Date of Initial Production:	May 21, 2004

III. Packaging Information

A. Package Type:	36-pin TQFN 6x6	36-bump WLP
B. Lead Frame:	Copper	N/A
C. Lead Finish:	100% matte Tin	N/A
D. Bondwire:	Au (1 mil dia.)	N/A (N/A mil dia.)
E. Mold Material:	Epoxy with silica filler	None
F. Assembly Diagram:	#05-9000-0681	#05-9000-4352
G. Flammability Rating:	Class UL94-V0	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
I. Single Layer Theta Ja:	38°C/W	N/A°C/W
J. Single Layer Theta Jc:	1.4°C/W	N/A°C/W
K. Multi Layer Theta Ja:	28°C/W	38°C/W
L. Multi Layer Theta Jc:	1.4°C/W	N/A°C/W

IV. Die Information

A. Dimensions:	122X122 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83 \text{ (Chi square value for MTTF upper limit)}}{1000 \times 2454 \times 180 \times 2}$$

(where 2454 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 2.07 \times 10^{-9}$

$\lambda = 2.07$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the E35 Process results in a FIT Rate of 0.68 @ 25C and 11.68 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AS27-3 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX4761ETX+T / MAX4761EWX+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 125C Biased Time = 1000 hrs.	DC Parameters & functionality	180	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.