RELIABILITY REPORT

FOR

MAX4691ExE

PLASTIC ENCAPSULATED/CHIP SCALE DEVICES

April 30, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX4691 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4691 are low-voltage CMOS analog ICs configured as an 8-channel Multiplexer.

The MAX4691 operates from either a single +2V to +11V power supply or dual ±2V to ±5.5V power supplies. When operating from ±5V supplies it offers 25Ω on-resistance (R_{ON}), 3.5Ω (max) R_{ON} flatness, and 3Ω (max) matching between channels.

All digital inputs are 1.8V logic-compatible when operating from a +3V supply and TTL compatible when operating from a +5V supply.

The MAX4691 is available in 16-pin, 4mm x 4mm QFN and 16-bump UCSP packages. The chip-scale package (UCSP™) occupies a 2mm x 2mm area, significantly reducing the required PC board area.

B. Absolute Maximum Ratings

Item	Rating
V+ to GND	-0.3V to +12V
V+ to V-	-0.3V to +12V
Voltage into any Terminal (Note 1)	(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into any Terminal	±20mA
Peak Current W_, X_, Y_, Z_ (pulsed at 1ms,10% duty cycle)	±40mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering)	
16-Bump UCSP (Note 2) Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C
16-Pin QFN	+300°C
Continuous Power Dissipation	
16-Lead QFN	1481mW
16-Bump UCSP	659mW
Derates above +70°C	
16-Lead QFN	18.5mW/°C
16-Bump UCSP	8.3mW/°C

Note 1: Voltages exceeding V+ or V- on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.
Note 2: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow.

II. Manufacturing Information

A. Description/Function:	Low-Voltage 8:1 Multiplexer
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	292
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea or USA
F. Date of Initial Production:	January, 2001

III. Packaging Information

	16-Lead QFN (4x4)	**16-Bump UCSP**
A. Package Type:		
B. Lead Frame:	Copper	N/A
C. Lead Finish:	Solder Plate	N/A
D. Die Attach:	Non-Conductive Epoxy	N/A
E. Bondwire:	Gold (1 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	N/A
G. Assembly Diagram:	# 05-1201-0217	# 05-1201-0216
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	80 x 80 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 77 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 14.10 \times 10^{-9}$

$\lambda = 14.10$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5702) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AH75 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4691ExE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		77	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN UCSP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	QFN UCSP	77 N/A	0 N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010 (Note 3)	DC Parameters	QFN UCSP	77 77	0 0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: UCSP Temperature Cycle performed at -40 ° C/125 ° C, 1000 Cycles, ramp rate 11 ° C/minute, dwell=15 minutes, One cycle/hour

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

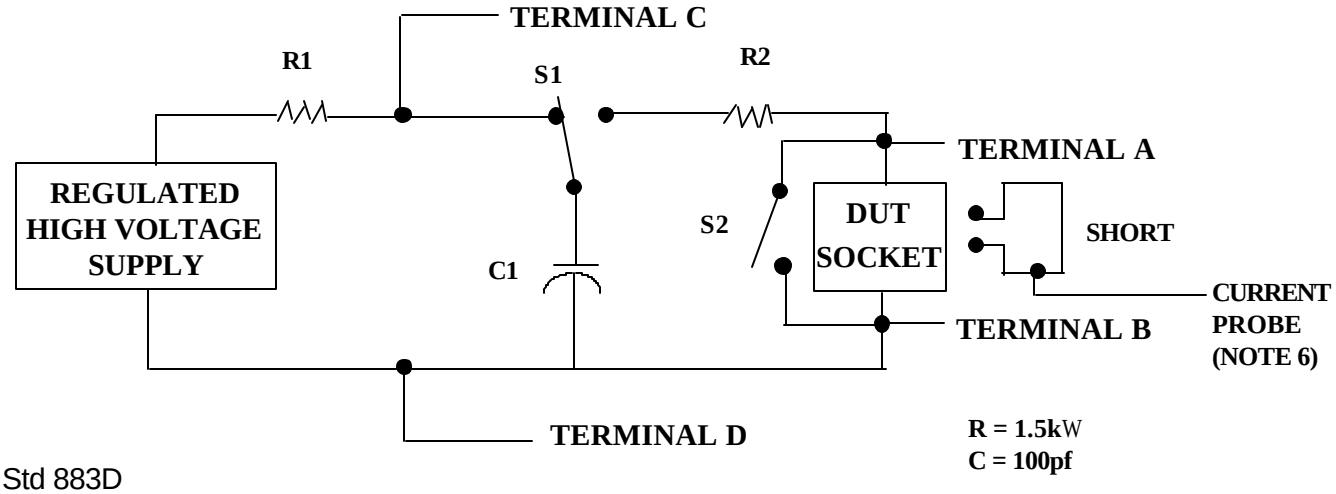
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

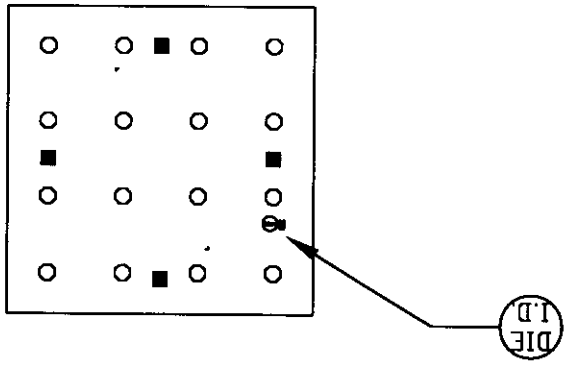
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

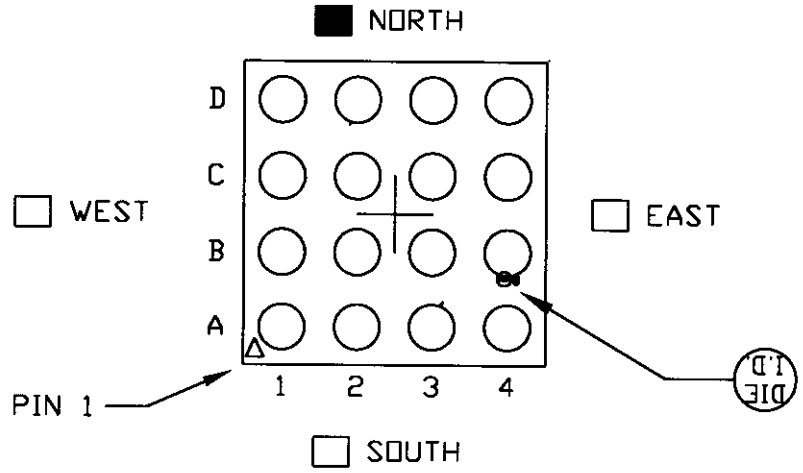


Mil Std 883D
Method 3015.7
Notice 8

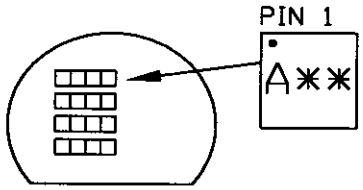
ORIGINAL CHIP



AFTER BUMP

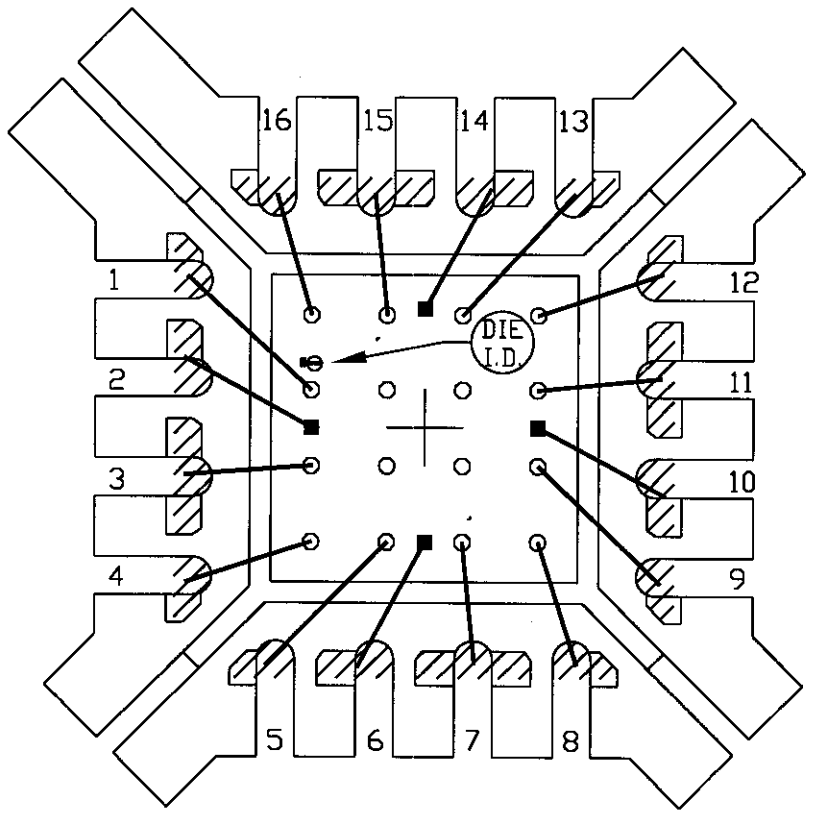


SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.



PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)

PKG. CODE: B16-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: N/A	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0216 / REV: B



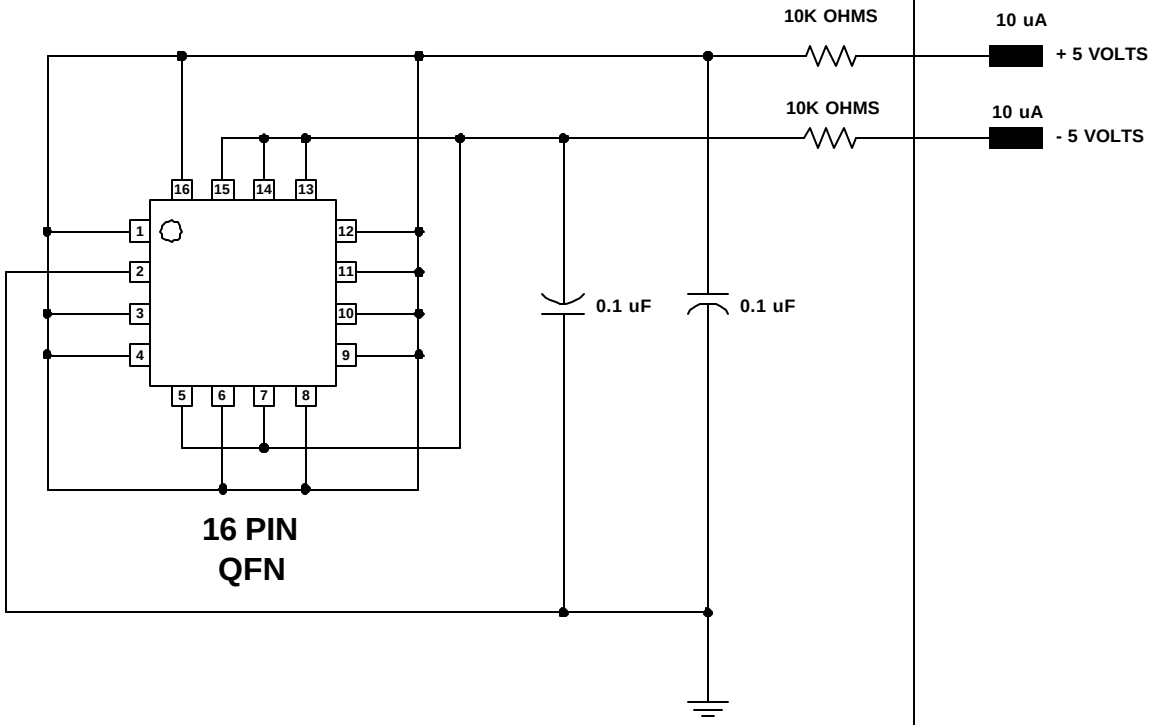
BONDABLE AREA

PKG. BODY SIZE: 4x4 mm

PKG. CODE: G1644-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 91x91	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0217 / REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 4691, 4692, 4693

MAX. EXPECTED CURRENT = (+/- 5 v) 10 uA

NOTES: