RELIABILITY REPORT

FOR

MAX4648EUT

PLASTIC ENCAPSULATED DEVICES

October 18, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX4648 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4648 is a dual-supply single-pole/single-throw (SPST) switch. On-resistance is 25Ω max and flat (2Ω max) over the specified signal range. The switch can handle Rail-to-Rail® analog signals. Off-leakage current is only 1nA max at +25°C. It conducts analog or digital signals equally well in either direction. The primary application areas are in the switching and routing of signals in telecommunications and test equipment.

The MAX4648 is single SPST analog switches with one normally open (NO) switch. This device operates from a single +9V to +36V supply or from dual ±4.5V to ±20V supplies. The MAX4648 are available in tiny 6-pin SOT23 packages.

B. Absolute Maximum Ratings

Item	Rating
(Voltages referenced to GND)	
V+	-0.3V, +44.0V
V-	-44.0V, +0.3V
V+ to V-	-0.3V to +44.0V
All Other Pins (Note 1)	V- - 0.3V to V+ + 0.3V
Continuous Current into Any Terminal	±60mA
Peak Current into Any Terminal (pulsed at 1ms, 10% duty cycle)	±100mA
Operating Temperature Ranges	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
6-Pin SOT23	696mW
Derates above +70°C	
6-Pin SOT23	8.7mW/°C

Note 1: Signals on NO, NC, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current tomaximum current rating.

II. Manufacturing Information

A. Description/Function:	25 Ohm SPST Analog Switches in SOT23-6
B. Process:	S5HV/MV2 – Medium Voltage 5 micron silicon gate CMOS
C. Number of Device Transistors:	24
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia or Thailand
F. Date of Initial Production:	January, 2001

III. Packaging Information

A. Package Type:	**6-Pin SOT23**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Non-Conductive Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1201-0214
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	37 x 59 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contact: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5696) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AH57-1 die type has been found to have all pins able to withstand a transient pulse of <100V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA and/or ±20V.

Table 1

Reliability Evaluation Test Results

MAX4648EUT

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	SOT	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

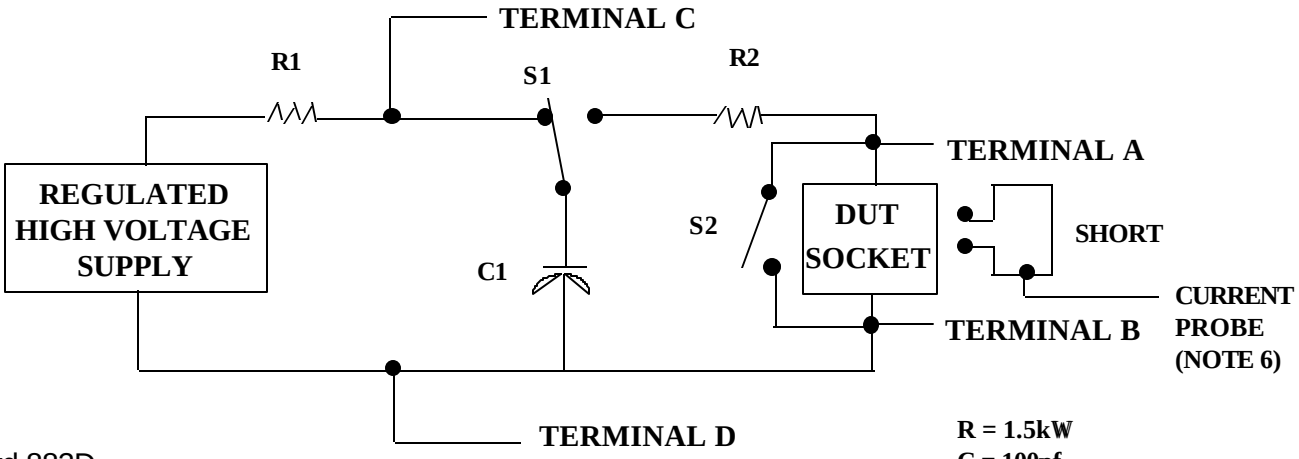
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

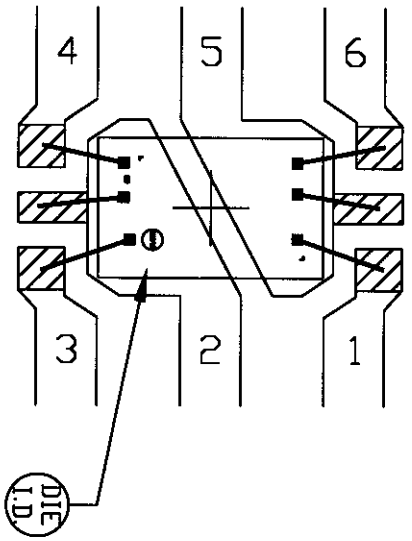
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



USE NON-CONDUCTIVE EPOXY

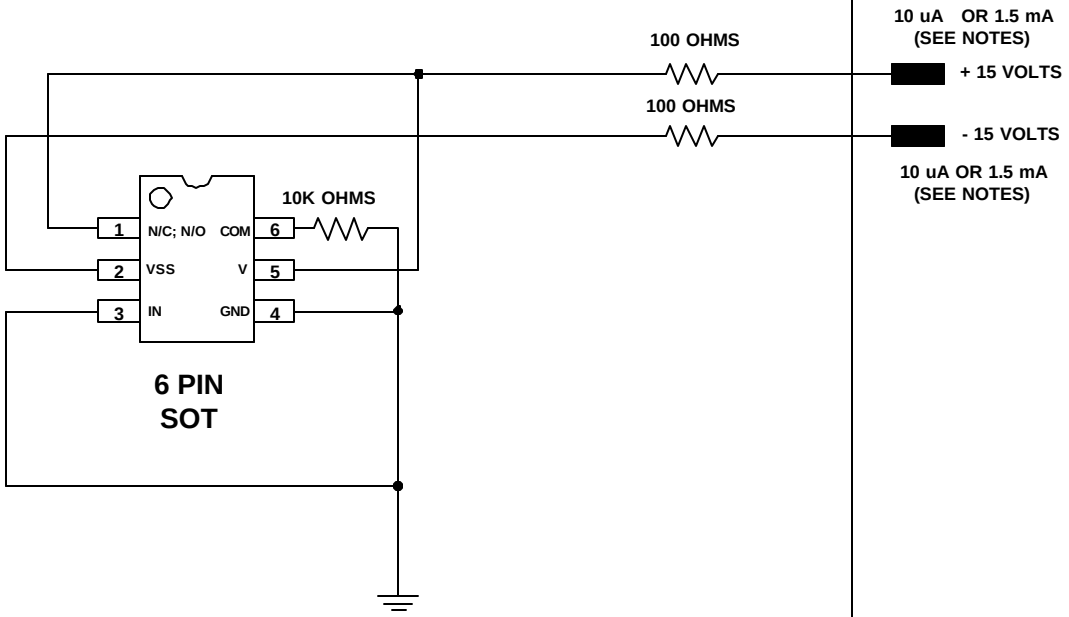
NOTE: USE NON-CONDUCTIVE EPOXY ONLY

BONDABLE AREA

PKG. CODE: U6S-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 64x46	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0214 / REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 4647 / 8

MAX. EXPECTED CURRENT = (+/- 15V) 10uA OR 1.5 mA; SEE NOTES.

NOTES: 1) MAX4647 CURRENT WHEN SWITCH IS CLOSED IS 1.5 mA.
2) MAX4648 CURENT WHEN SWITCH IS OPEN IS 10 uA.
3) +/- 15V, SUPPLIES USES EITHER CURRENT DEPENDING ON WHICH DEVICES ARE BEING LOADED