

RELIABILITY REPORT  
FOR  
**MAX4632xxE**  
PLASTIC ENCAPSULATED DEVICES

August 16, 2002

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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## Conclusion

The MAX4632 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX4632 high-voltage, dual analog switch is pin compatible with the industry-standard DG403. It upgrade's the existing device with fault-protected inputs and Rail-to-Rail<sup>®</sup> signal handling capabilities. The MAX4632's normally open (NO) and normally closed (NC) terminals are protected from overvoltage faults up to 36V during power-up or power-down. During a fault condition, these terminals become open circuit and only nanoamperes of leakage current flow from the source, yet the switch output (COM\_) continues to furnish up to 18mA of the appropriate polarity supply voltage to the load. This ensures unambiguous rail-to-rail outputs when a fault begins and ends. On-resistance is 85 $\Omega$  (max) at +25°C and is matched between switches to 6 $\Omega$  (max). Off-leakage current is only 0.5nA at +25°C and 5nA at +85°C.

The MAX4632 has two NO/NC single-pole/double-throw (SPDT) switches.

This CMOS switch operates with dual power supplies ranging from  $\pm 4.5V$  to  $\pm 18V$  or a single supply between +9V and +36V. All digital inputs have +0.8V and +2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using  $\pm 15V$  or a single +12V supply.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
(Voltages referenced to GND)	
V+	-0.3V to +44V
V-	-44V to +0.3V
V+ to V-	-0.3V to +44V
COM_, IN_ (Note 1)	(V- - 0.3V) to (V+ + 0.3V)
NC_, NO_ (Note 2)	(V+ - 25V) to (V- + 25V)
NC_, NO_ to COM_	+25V
Continuous Current into Any Terminal	$\pm 30mA$
Peak Current into Any Terminal (pulsed at 1ms, 10% duty cycle)	$\pm 50mA$
Operating Temperature Ranges	
MAX4632CxE	0°C to +70°C
MAX4632ExE	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +70°C) (Note 2)	
16 Lead PDIP	842mW
16 Lead NSO	696mW
Derates above +70°C	
16 Lead PDIP	10.53mW/°C
16 Lead NSO	8.70mW/°C

Note 1: Signals on NC\_, NO\_, COM\_, or IN\_ exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current rating.

Note 2: All leads are soldered or welded to PC board.

## II. Manufacturing Information

A. Description/Function:	Fault-Protected, High-Voltage, Dual Analog Switches
B. Process:	S5 (SG5) - Standard 5 micron silicon gate CMOS
C. Number of Device Transistors:	223
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines or Malaysia
F. Date of Initial Production:	July, 1999

## III. Packaging Information

A. Package Type:	<b>16 Lead NSO</b>	<b>16 Lead PDIP</b>
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1201-0098	Buildsheet # 05-1201-0097
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

## IV. Die Information

A. Dimensions:	86 x 128 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contact: Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 160 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 6.79 \times 10^{-9} \quad \lambda = 6.79 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-1727) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The AH21-1 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$  and/or  $\pm 20\text{V}$ .

**Table 1**

## Reliability Evaluation Test Results

**MAX6432xxE**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	PDIP	77	0
			NSO	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

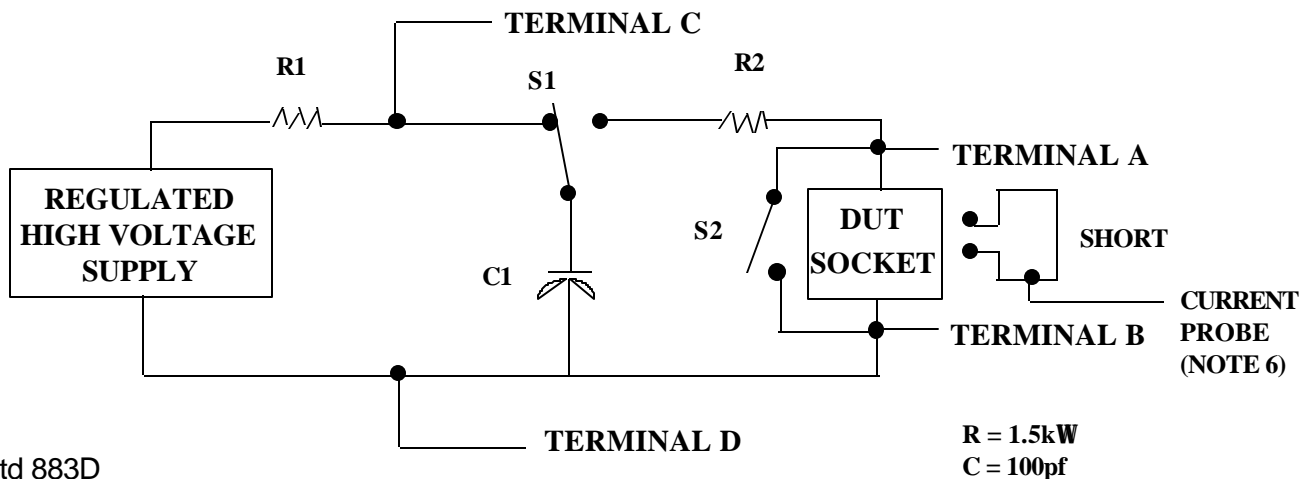
2/ No connects are not to be tested.

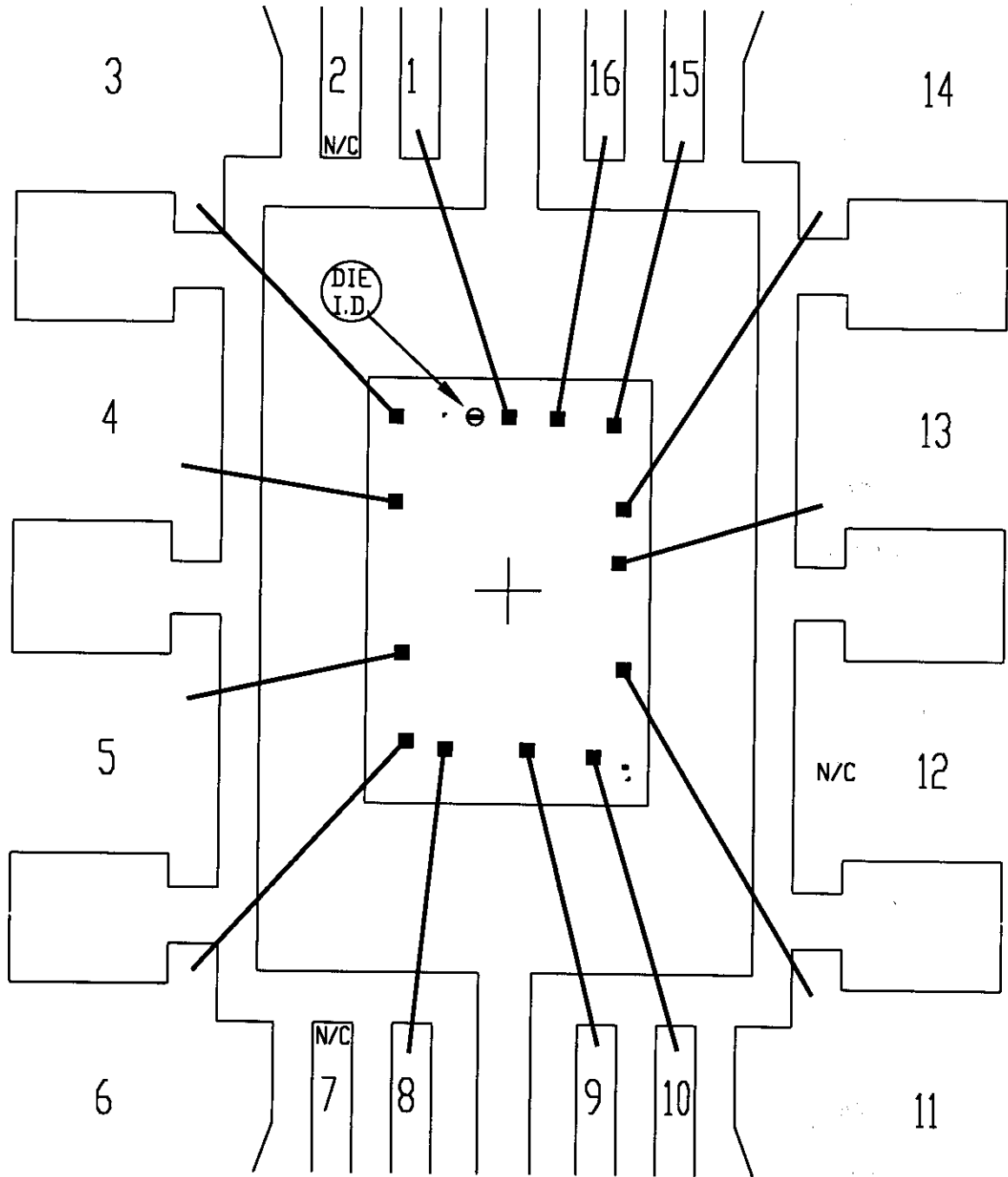
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.





PKG.CODE: P16-4

CAV./PAD SIZE:  
150 X 230

PKG.  
DESIGN

APPROVALS

DATE

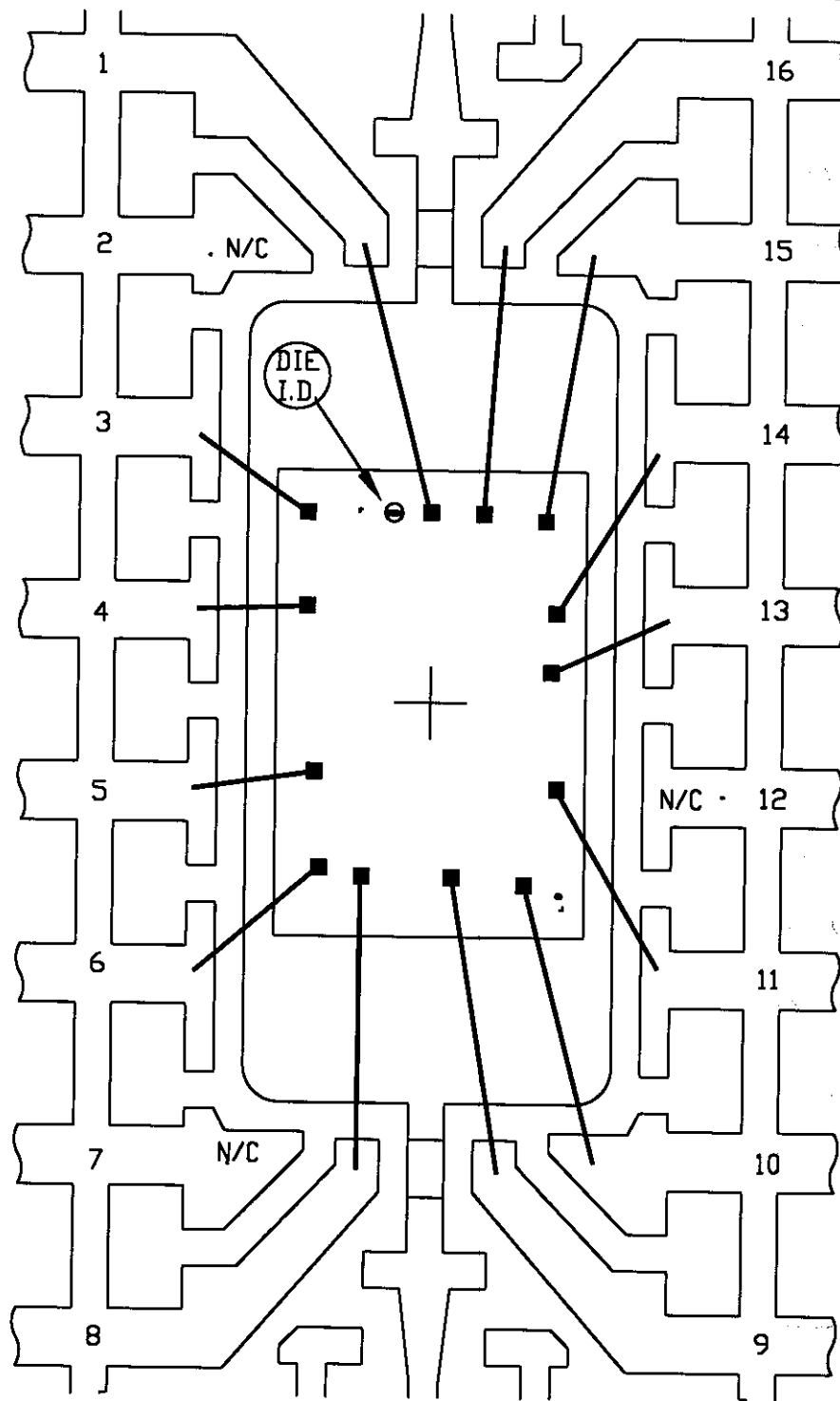
**MAXIM**

BUILDSHEET NUMBER:

REV.:

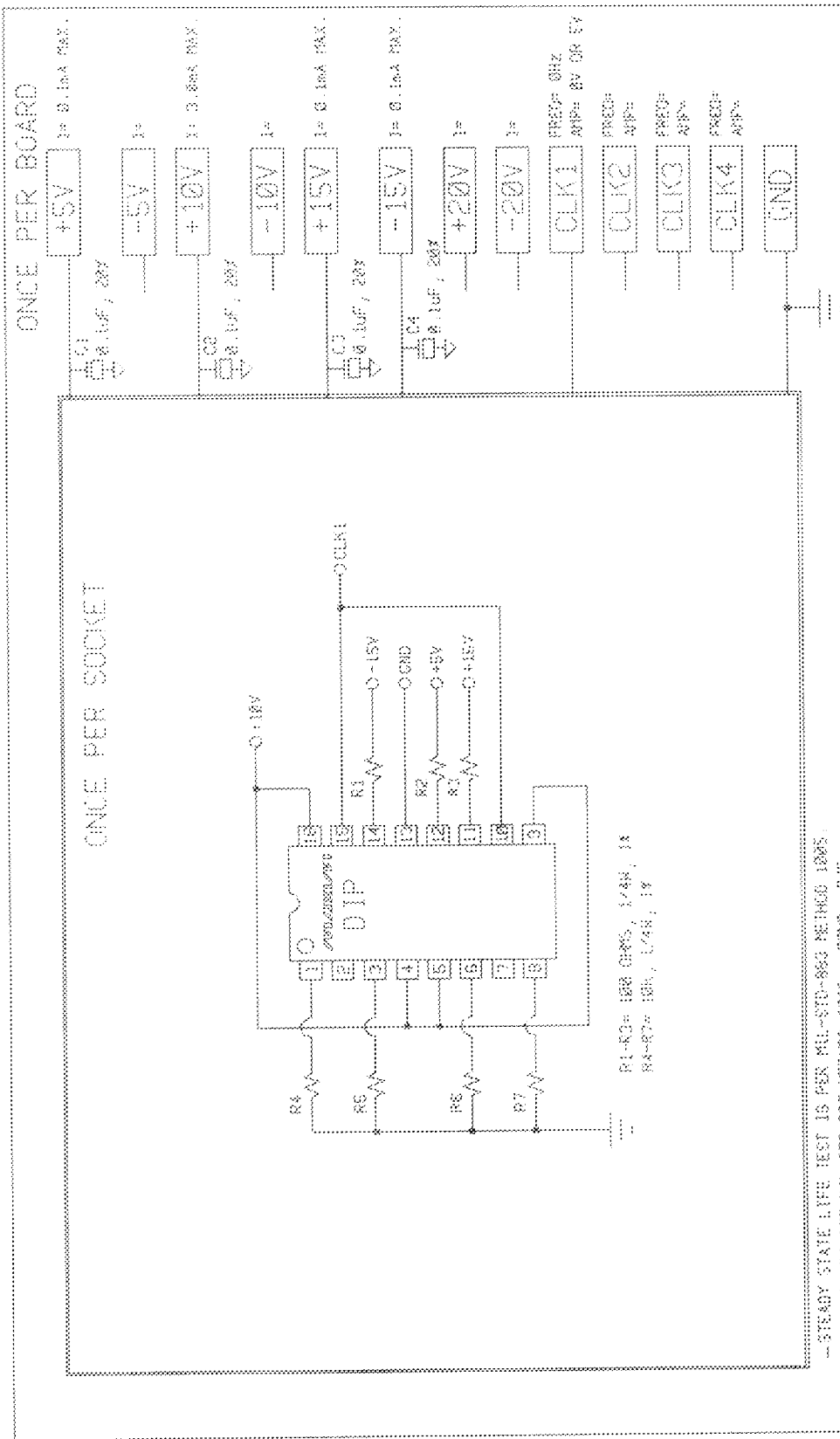
05-1201-0097

A



PKG.CODE: S16-8		APPROVALS	DATE	<b>MAXIM</b>	
CAV./PAD SIZE: 102X220	PKG. DESIGN			BUILDSHEET NUMBER: 05-1201-0098	REV: A





STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005  
 BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B/C

SPEC. NO. 06-1727 REV. E	MAX IM BURN-IN SCHEMATIC	SERVICE TYPE: DC564/SR, 1HE042/1/2/3/4/5/7/6/5 1H5858/1, 1H5142/1/2/3/4/5/7/5 HAK381/383/385 80-88 L/483/485
NOTES:	DATE: 4/26/95	1. TEMPERATURE: 100C OR EQUIVALENT 2. TIME: 150 HOURS MIN. OR EQUIVALENT 3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS 4. APPROVED FOR (X) COMMERCIAL (X) MR/880