RELIABILITY REPORT

FOR

MAX4617xxx

PLASTIC ENCAPSULATED DEVICES

October 23, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
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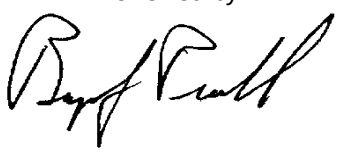
Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX4617 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4617 is a high-speed, low-voltage, CMOS analog IC configured as an 8-channel multiplexer.

This CMOS device can operate continuously with a +2V to +5.5V single supply. Each switch can handle Rail-to-Rail® analog signals. The off-leakage current is only 1nA at T_A = +25°C and 10nA at T_A = +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply.

B. Absolute Maximum Ratings

Item	Rating
Voltages Referenced to GND	
VCC, A, B, C, or Enable	-0.3V to +6V
Voltage into Any Analog Terminal (Note 1)	-0.3V to (VCC + 0.3V)
Continuous Current into Any Terminal	±75mA
Peak Current, X_, Y_, Z_ (pulsed at 1ms, 10% duty cycle)	±200mA
Operating Temperature Ranges	
MAX4617C_ _	0°C to +70°C
MAX4617E_ _	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16 Lead TSSOP	533mW
16 Lead QFN	1481mW
16 Lead NSO	696mW
16 Lead PDIP	842mW
Derates above +70°C	
16 Lead TSSOP	6.7mW/°C
16 Lead TSSOP	18.5mW/°C
16 Lead TSSOP	8.70mW/°C
16 Lead TSSOP	10.53mW/°C

Note 1: Voltages exceeding VCC or GND on any analog signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function:	High-Speed, Low-Voltage, CMOS Analog Multiplexers
B. Process:	T06 (0.6 micron TSMC CMOS)
C. Number of Device Transistors:	244
D. Fabrication Location:	Taiwan, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	July, 1999

III. Packaging Information

A. Package Type:	**16 Lead TSSOP**	**16-Lead QFN**	**16-Lead NSO**
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1.2 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0132	# 05-1201-0275	# 05-1201-0113
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

A. Package Type:	**16 Lead PDIP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0110
J. Flammability Rating:	Class UL94-V0
K. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	72 x 63 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si/Cu (Aluminum/ Silicon/ Copper)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal 1: 0.9 microns; Metal 2: 0.9 microns (as drawn)
F. Minimum Metal Spacing:	Metal 1: 0.8 microns; Metal 2: 0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AH24 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX4617xxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO PDIP TSSOP QFN	77 77 77 77	0 0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Process/Package Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

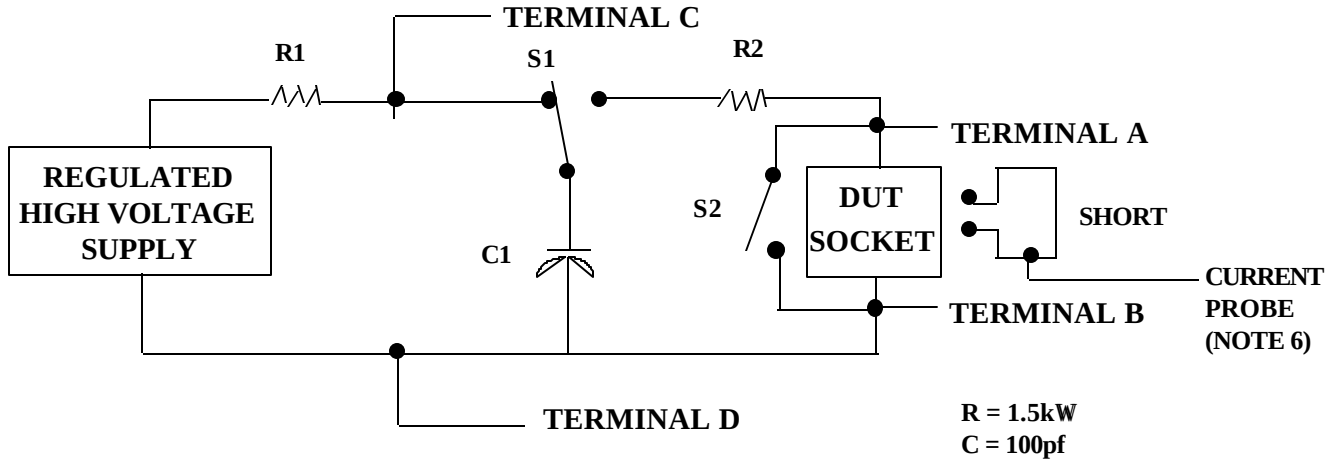
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

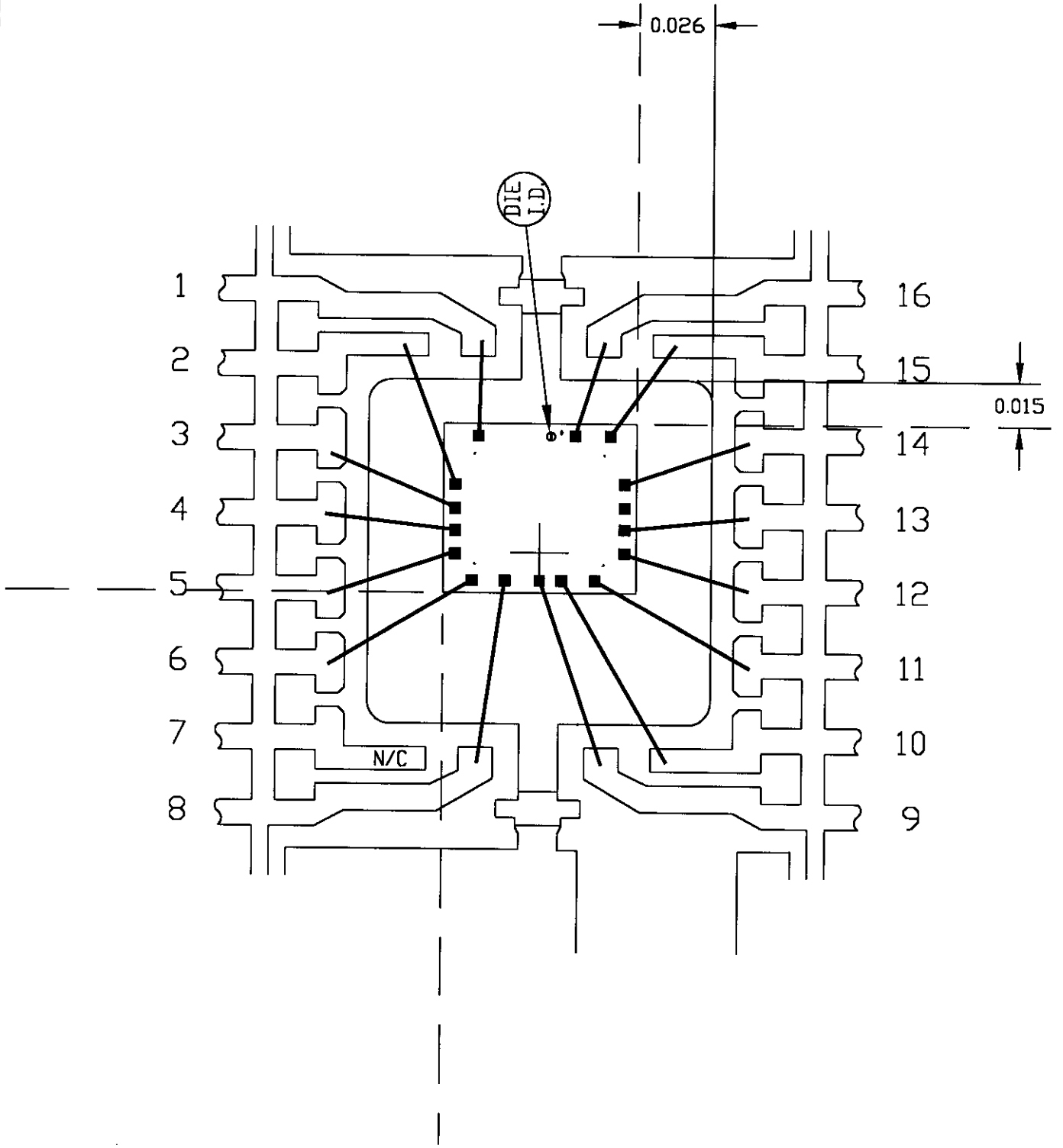
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

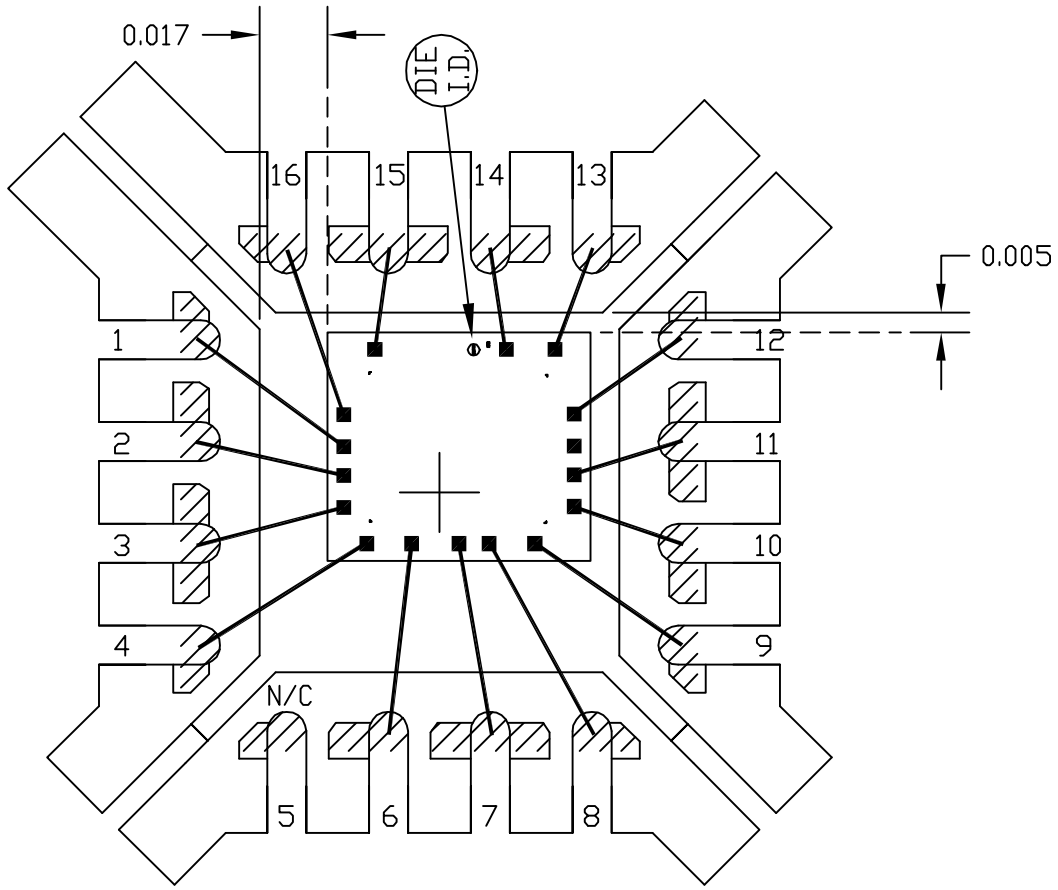
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: U16-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 118X118	PKG. DESIGN			BUILDSHEET NUMBER: 05-1201-0132 / REV.: A

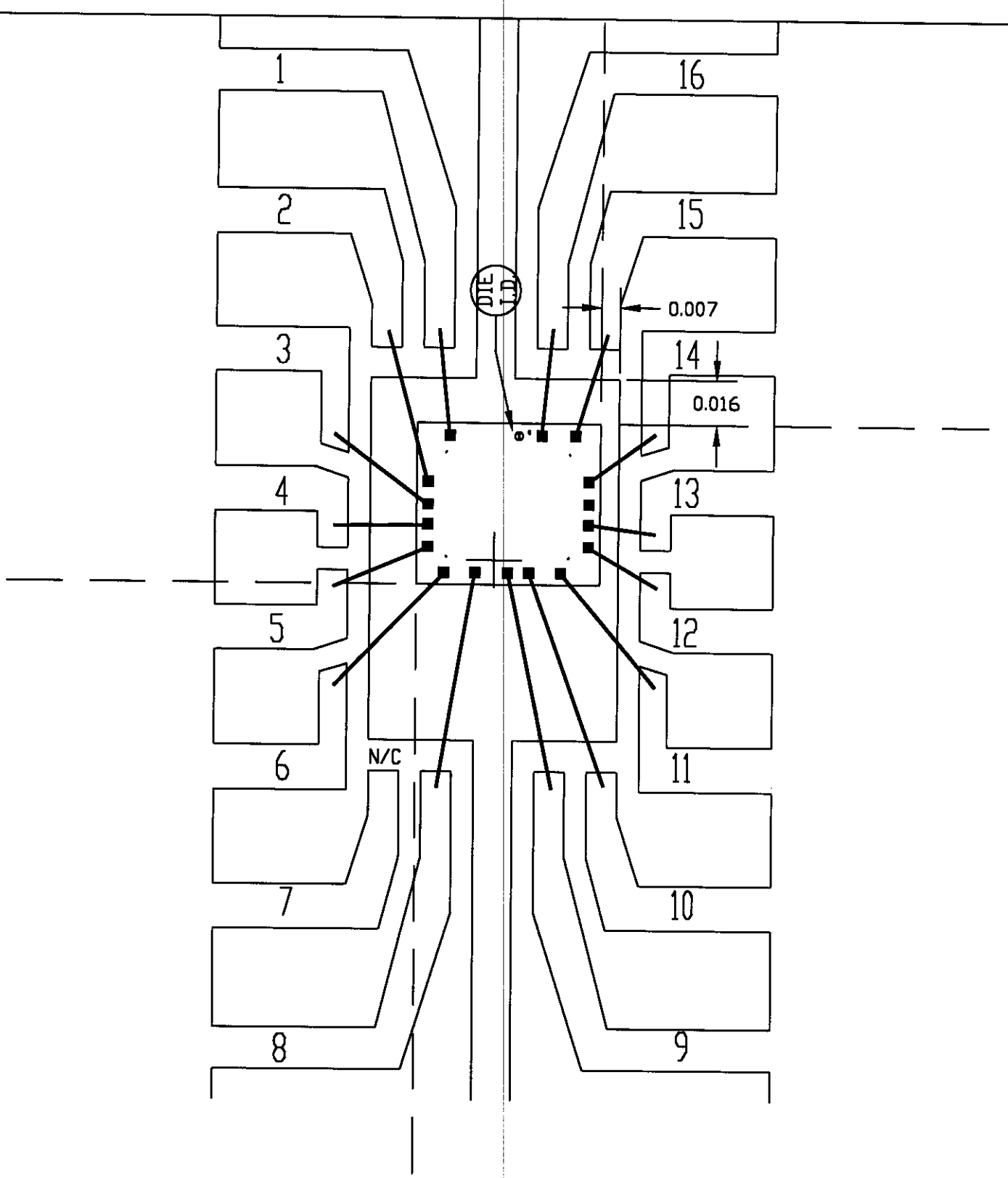
EXPOSED PAD PKG.



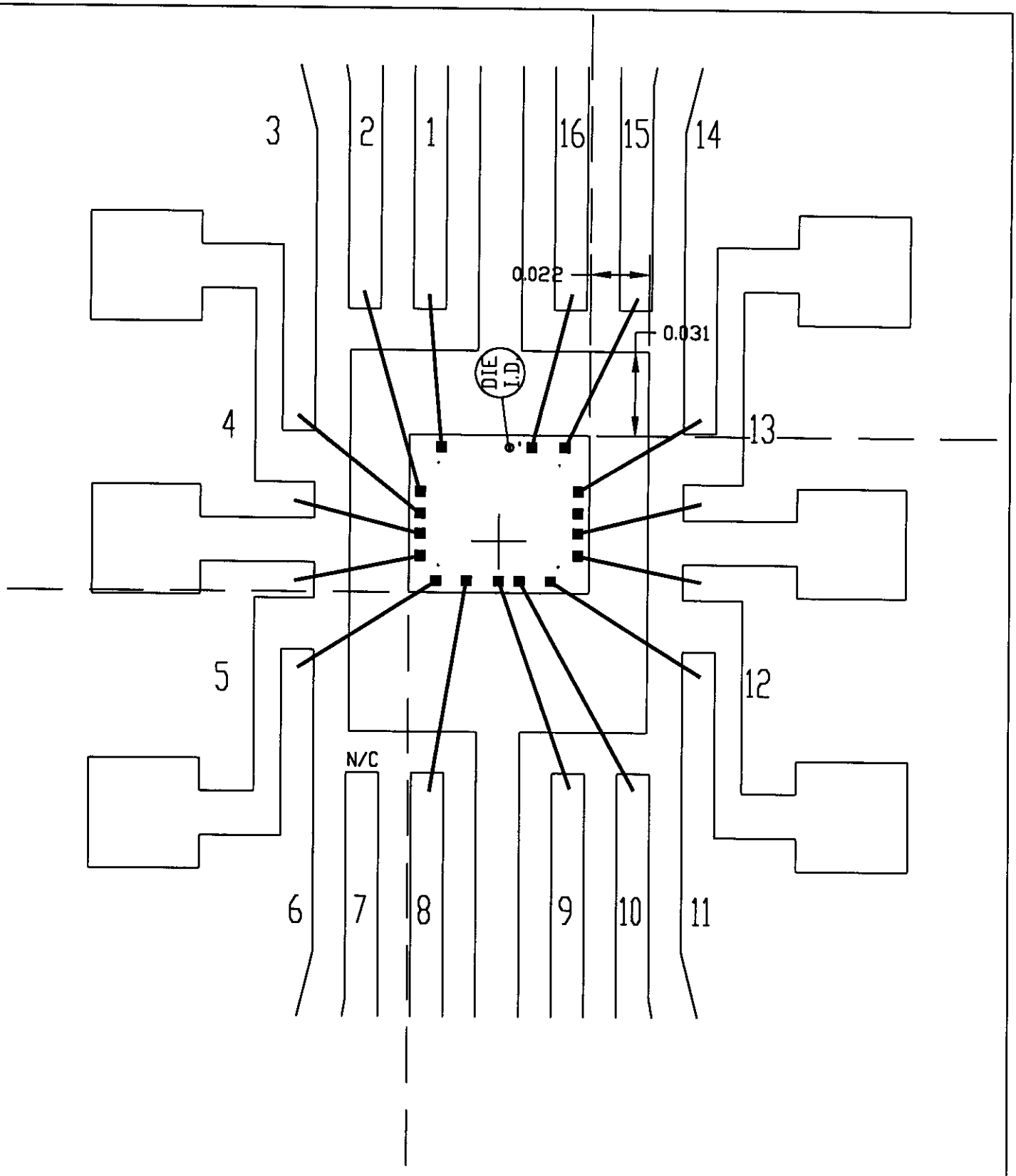
BONDABLE AREA

PKG. BODY SIZE: 4x4 mm

PKG. CODE: G1644-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 91x91	PKG.			BOND DIAGRAM #: 05-1201-0275	REV: A
	DESIGN				



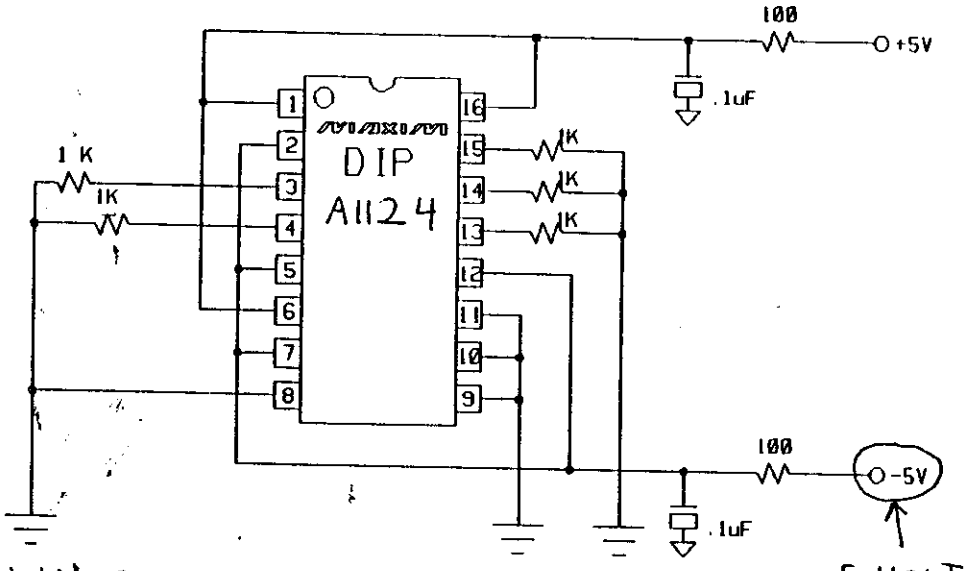
PKG.CODE: S16-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 90 X 130	PKG. DESIGN			BUILDSHEET NUMBER: 05-1201-0113 / REV.: A



PKG.CODE: P16-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 110 X 140	PKG. DESIGN			BUILDSHEET NUMBER: 05-1201-0110 / REV.: A

ONCE PER BOARD

ONCE PER DEVICE



*USES BURN-IN BOARD FOR MAX 4051/52/53 (06-5145)

-5 VOLT PIN MUST BE JUMPED TO GND FOR AH24

+5V I < 1uA

100uF

GND I < 1uA

100uF

PS3 I =

PS4 I=

PS5 I =

PS6 I =

CLK0 FREQ= AMP=

CLK1 FREQ= AMP=

CLK2 FREQ= AMP=

CLK3 FREQ= AMP=

CLK4 FREQ= AMP=

GND

-STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
-BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MR/883

SPEC. NO.* 06-5484 REV: A

DATE: 6/18/99

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S): (AH24)

MAX4617/18/19