

RELIABILITY REPORT FOR

MAX4526EUA+

PLASTIC ENCAPSULATED DEVICES

October 3, 2012

## **MAXIM INTEGRATED**

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Approved by
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#### Conclusion

The MAX4526EUA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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## I. Device Description

A. General

The MAX4526/MAX4527 are CMOS analog ICs configured as phase-reversal switches. The MAX4526 is optimized for high-speed applications, such as chopper amplifiers, while the MAX4527 is optimized for low-power applications. The MAX4526/MAX4527 operate from a +4.5V to +36V single supply or ±4.5V to ±18V dual supplies. On-resistance (175 max) is matched between switches to 8 maximum. Each switch can handle rail-to-rail analog signals. Maximum leakage current is only 0.5nA at +25°C and 10nA at +85°C. All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility.



#### II. Manufacturing Information

A. Description/Function: Phase-Reversal Analog Switches

B. Process: S5

C. Number of Device Transistors:

D. Fabrication Location: Oregon

E. Assembly Location: Philippines, Thailand, Malaysia

F. Date of Initial Production: Pre 1997

## III. Packaging Information

A. Package Type: 8-pin uMAX
B. Lead Frame: Copper

C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-0301-0802
H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per

JEDEC standard J-STD-020-C

Level 1

J. Single Layer Theta Ja: 221°C/W K.
Single Layer Theta Jc: 41.9°C/W
L. Multi Layer Theta Ja: 206.3°C/W
M. Multi Layer Theta Jc: 41.9°C/W

## IV. Die Information

A. Dimensions: 58 X 77 mils

B. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier

D. Backside Metallization: None

E. Minimum Metal Width: 5.0 microns (as drawn)F. Minimum Metal Spacing: 5.0 microns (as drawn)

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO<sub>2</sub>I. Die Separation Method: Wafer Saw



#### V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)

Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm
D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

#### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\chi = 6.1 \times 10^{-9}$$

3. = 6.1 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S5 Process results in a FIT Rate of 0.09 @ 25C and 1.55 @ 55C (0.8 eV, 60% UCL)

## B. E.S.D. and Latch-Up Testing (ESD lot NQYABQ002D D/C 0038, Latch-Up lot XQYAAX001D D/C 9644)

The AG90 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-100mA.



# **Table 1**Reliability Evaluation Test Results

## MAX4526EUA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test	(Note 1)				
	Ta = 135°C	DC Parameters	50	0	NQYABQ002J, D/C 0101
	Biased	& functionality	80	0	XQYAAX001D, D/C 9644
	Time = 192 hrs.	·	50	0	XQYBAX001C, D/C 9644

Note 1: Life Test Data may represent plastic DIP qualification lots.