

RELIABILITY REPORT
FOR
MAX4473ExA
PLASTIC ENCAPSULATED DEVICES

March 29, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX4473 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4473 PA power control IC is intended for closed-loop bias control of GSM power amplifiers. The device facilitates accurate control of the current delivered to the power amplifier (PA) via a control voltage. The error amplifier senses the voltage drop across an external current-sense resistor placed between the supply and the PA. The output of the error amplifier adjusts the PA gain until the current is proportional to the power control voltage applied to the MAX4473. This unique topology is useful in time-division-multiple-access (TDMA) systems, such as GSM, where accurate transmit burst shaping and power control is required. User-selectable current sensing and gain setting resistors maximize flexibility.

The MAX4473 operates from a single +2.7V to +6.5V supply and typically draws 1.2mA of supply current. The error amplifier has a common-mode range that extends from +1V to V_{CC} . The power control input and error amplifier outputs swing Rail-to-Rail®. A low-power shutdown mode reduces supply current to less than 1 μ A and activates an on-board active pull-down at the error amplifier output. Fast enable/disable times of 0.9 μ s reduce average power consumption without compromising dynamic performance. The MAX4473 is available in a space-saving 8-pin μ MAX package.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VCC to GND	7V
SR1, SR2, SR3, PC, /SHDN, OUT to GND	-0.3V to (VCC + 0.3V)
SR1 to SR3	0 to VCC
OUT and SR3 Short-Circuit Duration to VCC or GND	Continuous
OUT_ Short-Circuit Duration to VEE or VCC	10ns
Current into Any Pin	+/-50mA
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin uMAX	330mW
8-Pin QFN	1951mW
8-Pin NSO	471mW
Derates above +70°C	
8-Pin uMAX	4.1mW/°C
8-Pin QFN	24.4mW/°C
8-Pin NSO	5.88mW/°C

II. Manufacturing Information

A. Description:	Low-Cost, Low-Voltage. PA Control Amplifier for GSM Applications
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	348
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Korea, Thailand, Philippines or Malaysia
F. Date of Initial Production:	March, 1999

III. Packaging Information

A. Package Type:	8-Lead uMAX	8-Lead QFN	8-Lead NSO
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-3001-0133	# 05-3001-0185	# 05-3001-0132
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	53 x 44 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.57 \times 10^{-9} \quad \lambda = 13.57 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5390) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OP99 die type has been found to have all pins able to withstand a transient pulse of $\pm 1000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$ and/or $\pm 20\text{V}$.

Table 1
Reliability Evaluation Test Results

MAX4473ExA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX	360	0
			QFN	720	1
			NSO	1480	2
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test may represent DIP qualification packages.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

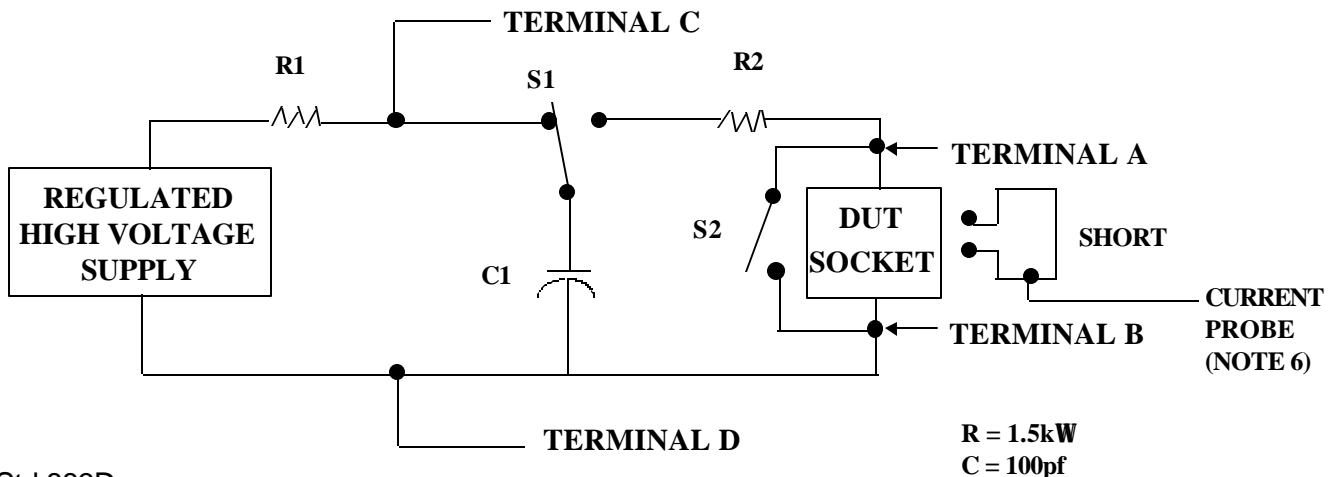
2/ No connects are not to be tested.

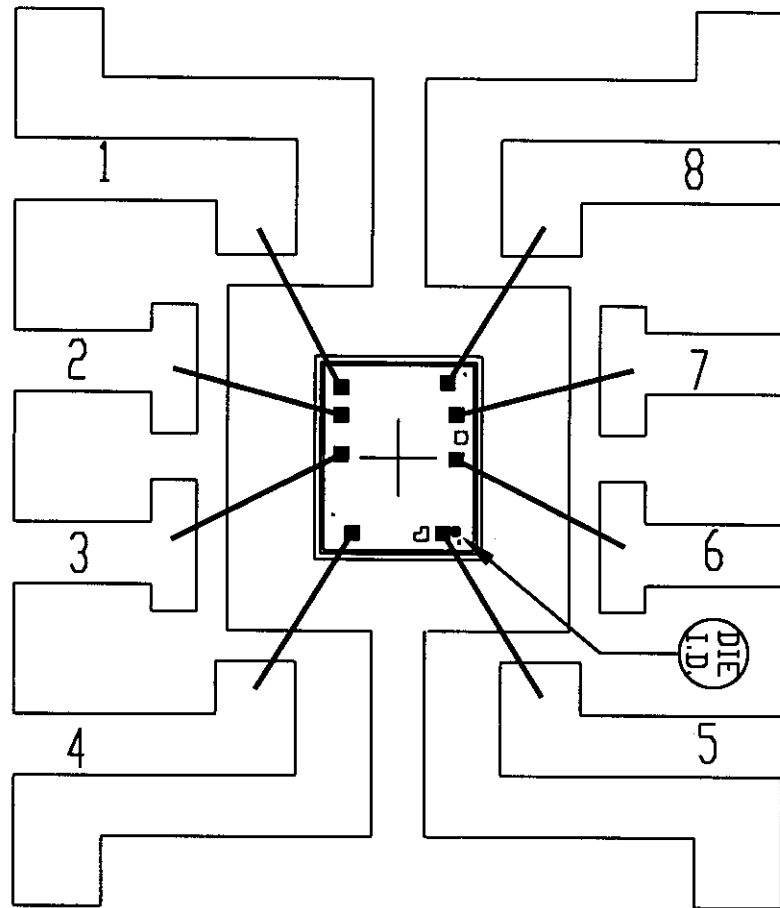
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





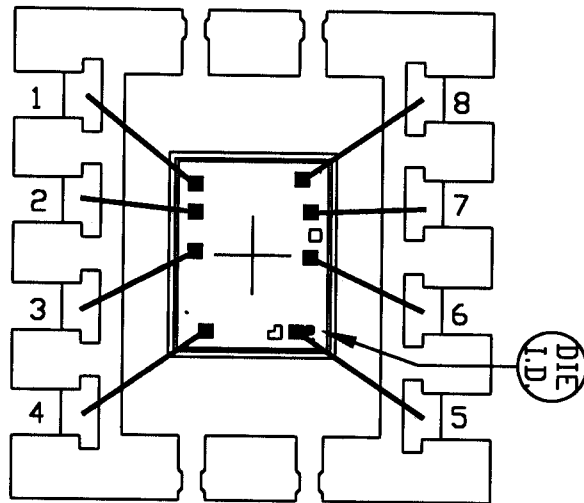
PKG.CODE: S8-2	
CAV./PAD SIZE: 90 X 90	PKG. DESIGN

APPROVALS

DATE



BUILDSHEET NUMBER: 05-3001-0132	REV.: A
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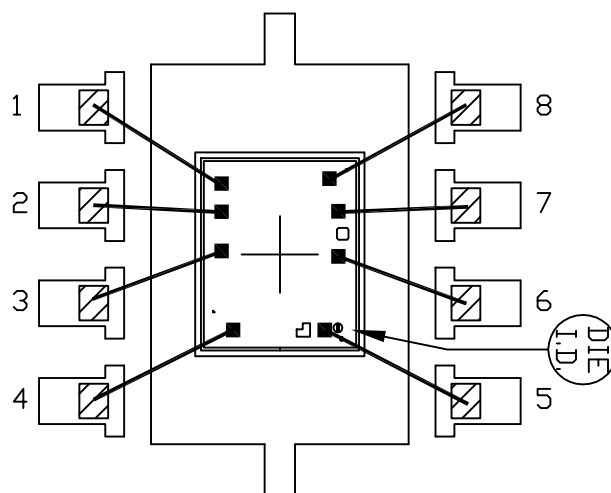
PKG.CODE:	U8-1
CAV./PAD SIZE:	68X94
	PKG. DESIGN

APPROVALS

DATE

MAXIM	
BUILDSHEET NUMBER:	REV.:
05-3001-0133	A

EXPOSED PAD PKG.



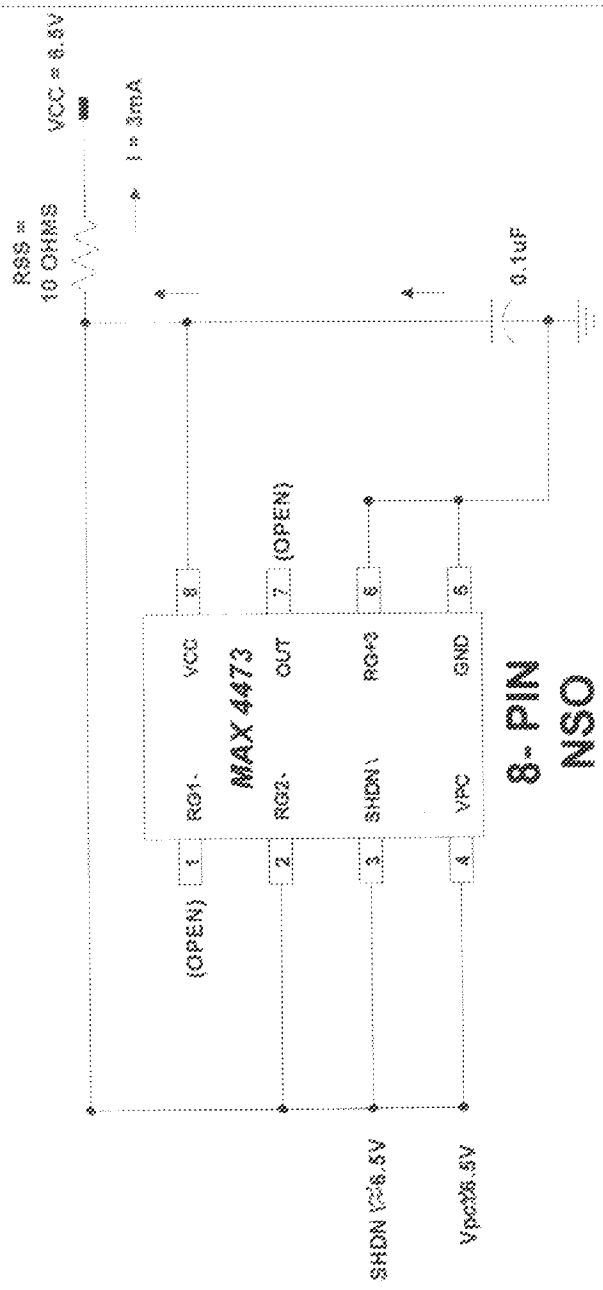
BONDABLE AREA

PKG. BODY SIZE: 3x3 mm

PKG. CODE: G833-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 67x99	PKG. DESIGN			BOND DIAGRAM #: 05-3001-0185	REV: B

ONCE PER SOCKET

ONCE PER BOARD



MAXIM BURN-IN SCHEMATIC
 SPEC 06-5390 REV. C
 DATE: 1 / 27 / 2000

DEVICES: MAX 4473
 MAX. EXPECTED CURRENT = 3mA

DRAWN BY:
 NOTES: PINS 1, 7; are open.