RELIABILITY REPORT

FOR

MAX4470ExK

PLASTIC ENCAPSULATED DEVICES

October 22, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord Quality Assurance Reliability Lab Manager Reviewed by

Bryan J. Preeshl Quality Assurance Executive Director

Conclusion

The MAX4470 sucessfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description

II.Manufacturing Information

III.Packaging Information

IV.Die Information

V.Quality Assurance Information

VI.Reliability Evaluation

VI.Reliability Evaluation

VI.Attachments

I. Device Description

A. General

The MAX4470 micropower op amp operates from a single +1.8V to +5.5V supply and draws only 750nA of supply current. The MAX4470 features ground-sensing inputs and Rail-to-Rail® outputs. The ultra-low supply current, low-operating voltage, and rail-to-rail output capabilities make this operational amplifier ideal for use in single lithium ion (Li+), or two-cell NiCd or alkaline battery systems.

The rail-to-rail output stage of the MAX4470 amplifier is capable of driving the output voltage to within 4mV of the rail with a $100k\Omega$ load, and can sink and source 11mA with a +5V supply. This amplifier is available in both fully compensated and decompensated versions. The single MAX4470 is unity-gain stable. This amplifier is available in space-saving SC70 and SOT23 packages.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
-------------	---------------

VDD to VSS -0.3V to +6V IN + or IN -(VSS - 0.3V) to (VDD + 0.3V)OUT_ Shorted to VSS or VDD Continuous Operating Temperature Range -40°C to +85°C Junction Temperature +150°C Storage Temperature Range -65°C to +150°C Lead Temperature (soldering, 10s) +300°C Continuous Power Dissipation (TA = $+70^{\circ}$ C) 5-Pin SC70 247mW 5-Pin SOT23 571mW Derates above +70°C 5-Pin SC70 3.1mW/°C 5-Pin SOT23 7.1mW/°C

II. Manufacturing Information

A. Description/Function: Single +1.8V/750nA, SC70, Rail-to-Rail Op Amps

B. Process: B8 (Standard 0.8 micron silicon gate CMOS)

C. Number of Device Transistors: 111

D. Fabrication Location: California, USA

E. Assembly Location: Philippines, Malaysia or Thailand

F. Date of Initial Production: April, 2001

III. Packaging Information

5-Lead SC70 5-Lead SOT23 A. Package Type: B. Lead Frame: Copper or Alloy 42 Copper C. Lead Finish: Solder Plate Solder Plate D. Die Attach: Silver-Filled Epoxy Silver-Filled Epoxy E. Bondwire: Gold (1.0 mil dia.) Gold (1.0 mil dia.) F. Mold Material: Epoxy with silica filler Epoxy with silica filler G. Assembly Diagram: # 05-2501-0065 # 05-2501-0066 H. Flammability Rating: Class UL94-V0 Class UL94-V0

Level 1

IV. Die Information

A. Dimensions: 31 x 30 mils

per JEDEC standard JESD22-A112: Level 1

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper

D. Backside Metallization: None

Classification of Moisture Sensitivity

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 158 \times 2}$$
 (Chi square value for MTTF upper limit)
$$\frac{1}{192 \times 4389 \times 158 \times 2}$$
 Thermal acceleration factor assuming a 0.8eV activation energy
$$\lambda = 6.87 \times 10^{-9}$$

$$\lambda = 6.87 \text{ F.I.T.}$$
 (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5662) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OX01 die type has been found to have all pins able to withstand a transient pulse of \pm 2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of \pm 250mA.

Table 1Reliability Evaluation Test Results

MAX4470ExK

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES	
Static Life Test	• (Note 1)					
Static Life Test	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		158	0	
Moisture Testin	ng (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT SC70	77 77	0 0	
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0	
Mechanical Str	Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)		
1.	All pins except V _{PS1} 3/	All V _{PS1} pins		
2.	All input and output pins	All other input-output pins		

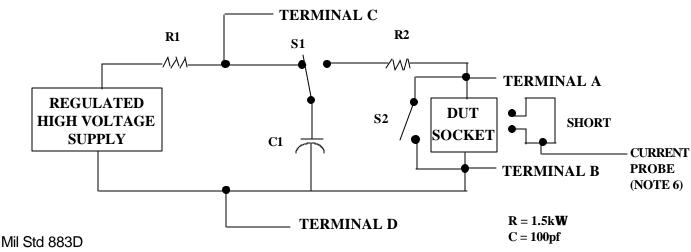
- Table II is restated in narrative form in 3.4 below.
- No connects are not to be tested.

 Repeat pin combination I for each named Power supply and for ground

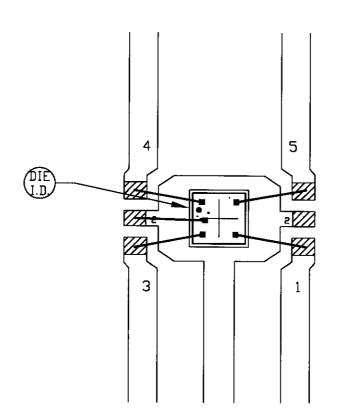
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected a. to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination b. of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of C. all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



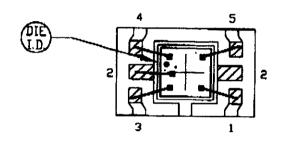
Method 3015.7 Notice 8



Ø- B□NDING AREA

NOTE:	CAV	ITY	$D\square WN$
· • —	\smile \cdot		

PKG. CODE: U5-1		SIGNATURES	DATE	CONFIDENTIAL & PROPRIE	
CAV./PAD SIZE:	PKG.			BOND DIAGRAM #:	REV:
64X45	DESIGN			05-2501-0066	Α

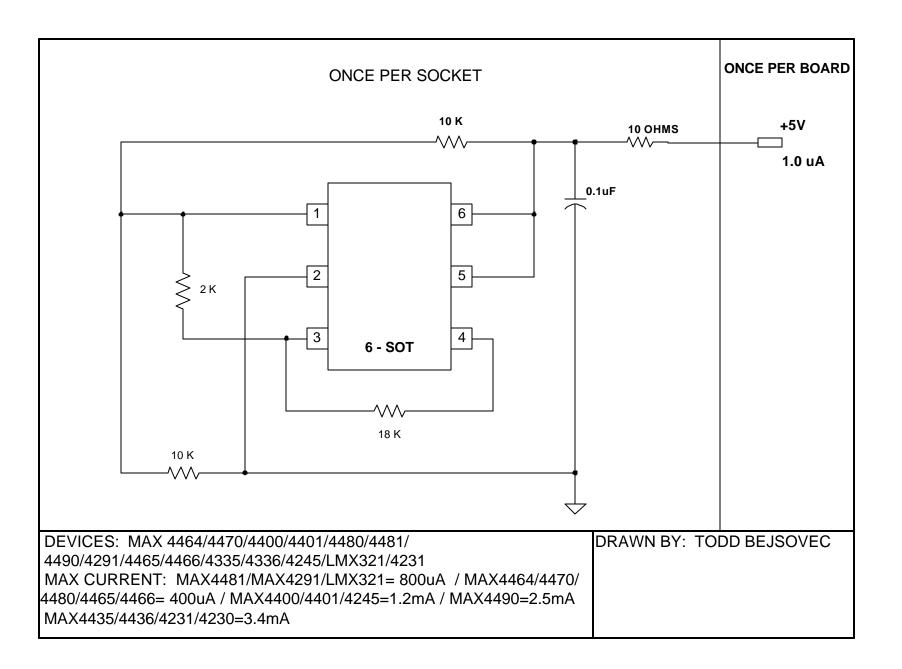


BUNDABLE AREA

NOTE: CAVITY DOWN

PKG. CODE: X5-1		SIGNATURES	DATE	CONFIDENTIAL & PROPRIE	TARY
CAV./PAD SIZE:	PKG.			BOND DIAGRAM #:	REV:
35×34	DESIGN			05-2501-0065	1 - 1

JOYCO'H JEJIZZZOGET



DOCUMENT I.D. 06-5662	REVISION E	MAXIM TITLE: BI Circuit (MAX4464/4470/4465/4466/4400/4401/4480/4481/4490/4291/4335/4336/4245/LMX321/	PAGE 2 OF 3
		4231/4230)	