

RELIABILITY REPORT  
FOR  
**MAX4428xxA**  
PLASTIC ENCAPSULATED DEVICES

October 13, 2002

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord  
Quality Assurance  
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl  
Quality Assurance  
Executive Director

## Conclusion

The [MAX4428](#) successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX4428 is a dual monolithic MOSFET driver designed to translate TTL/CMOS inputs to high voltage/current outputs. The MAX4428 is a MOSFET driver contains one inverting power section and one non-inverting section. Delay times are nearly independent of  $V_{DD}$ . High-current output drivers rapidly charge and discharge the gate capacitance of even the largest power MOSFETs to within millivolts of the supply rails. This produces the power MOSFET's minimum on resistance. The MAX4428's high speed minimizes power losses in switching power supplies and DC-DC converters.

#### B. Absolute Maximum Ratings

| <u>Item</u>                               | <u>Rating</u>                 |
|---|-------------------------------|
| Supply Voltage $V_{DD}$ to GND            | +20V                          |
| Input Voltage                             | $V_{DD} + 0.3V$ to GND - 0.3V |
| Storage Temp.                             | -65°C to +160°C               |
| Lead Temp. (10 sec.)                      | +300°C                        |
| Continuous Power Dissipation (TA = +70°C) |                               |
| 8-Lead DIP                                | 727mW                         |
| 8-Lead SO                                 | 471mW                         |
| Derates above +70°C                       |                               |
| 8-Lead DIP                                | 9.09mW/°C                     |
| 8-Lead SO                                 | 5.88mW/°C                     |

## II. Manufacturing Information

|                                  |   |
|----------------------------------|---|
| A. Description/Function:         | Dual High-Speed 1.5A MOSFET Driver        |
| B. Process:                      | SG5 (Standard 5 micron silicon gate CMOS) |
| C. Number of Device Transistors: | 26  |
| D. Fabrication Location:         | California, USA                           |
| E. Assembly Location:            | Philippines, Malaysia, or Thailand        |
| F. Date of Initial Production:   | April, 1992                               |

## III. Packaging Information

|   |                          |                          |
|---|--------------------------|--------------------------|
| A. Package Type:  | <b>8-Lead SO</b>         | <b>8-Lead PDIP</b>       |
| B. Lead Frame:  | Copper                   | Copper                   |
| C. Lead Finish:   | Solder Plate             | Solder Plate             |
| D. Die Attach:  | Silver-filled Epoxy      | Silver-filled Epoxy      |
| E. Bondwire:  | Gold (1.3 mil dia.)      | Gold (1.3 mil dia.)      |
| F. Mold Material:   | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram:  | # 05-0701-0588           | # 05-0701-0587           |
| H. Flammability Rating:   | Class UL94-V0            | Class UL94-V0            |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1                  | Level 1                  |

## IV. Die Information

|                            |   |
|----------------------------|---|
| A. Dimensions:             | 76 x 80 mils  |
| B. Passivation:            | Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide) |
| C. Interconnect:           | Aluminum/Si (Si = 1%)   |
| D. Backside Metallization: | None  |
| E. Minimum Metal Width:    | 5 microns (as drawn)  |
| F. Minimum Metal Spacing:  | 5 microns (as drawn)  |
| G. Bondpad Dimensions:     | 5 mil. Sq.  |
| H. Isolation Dielectric:   | SiO <sub>2</sub>  |
| I. Die Separation Method:  | Wafer Saw   |

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager-Reliability Operations)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 240 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 4.52 \times 10^{-9}$$

$$\lambda = 4.52 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-0555) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The PS28-5 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2500\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$  and/or  $\pm 20\text{V}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX4428xxA**

| TEST ITEM                         | TEST CONDITION  | FAILURE IDENTIFICATION           | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------|---|----------------------------------|---------|-------------|--------------------|
| <b>Static Life Test</b> (Note 1)  |   |                                  |         |             |                    |
|                                   | Ta = 135°C<br>Biased<br>Time = 192 hrs.                 | DC Parameters<br>& functionality |         | 240         | 0                  |
| <b>Moisture Testing</b> (Note 2)  |   |                                  |         |             |                    |
| Pressure Pot                      | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | SO      | 77          | 0                  |
|                                   |   |                                  | PDIP    | 77          | 0                  |
| 85/85                             | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs.      | DC Parameters<br>& functionality |         | 77          | 0                  |
| <b>Mechanical Stress</b> (Note 2) |   |                                  |         |             |                    |
| Temperature<br>Cycle              | -65°C/150°C<br>1000 Cycles<br>Method 1010               | DC Parameters                    |         | 77          | 0                  |

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic Process/Package Data

## Attachment #1

TABLE II. Pin combination to be tested. <sup>1/</sup> <sup>2/</sup>

|    | Terminal A<br>(Each pin individually connected to terminal A with the other floating) | Terminal B<br>(The common combination of all like-named pins connected to terminal B) |
|----|---|---|
| 1. | All pins except $V_{PS1}$ <sup>3/</sup>   | All $V_{PS1}$ pins  |
| 2. | All input and output pins   | All other input-output pins   |

<sup>1/</sup> Table II is restated in narrative form in 3.4 below.

<sup>2/</sup> No connects are not to be tested.

<sup>3/</sup> Repeat pin combination I for each named Power supply and for ground (e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

### 3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

