RELIABILITY REPORT

FOR

MAX4321EUK

PLASTIC ENCAPSULATED DEVICES

March 20, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX4321 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4321 operational amplifier (op amp) combines a 5MHz gain-bandwidth product and excellent DC accuracy with Rail-to-Rail® operation at both the inputs and the output. This device requires only 650μ A and operates from either a single +2.4V to +6.5V supply or dual ±1.2V to ±3.25V supplies, although the MAX4321 typically operates down to +1.8V (±0.9V). The MAX4321 remains unity-gain stable with capacitive loads up to 500pF and is capable of driving 250-ohm loads to within 200mV of either rail.

With rail-to-rail input common-mode range and output swing, the MAX4321 is ideal for low-voltage, single-supply applications. In addition, low ±1.2mV input offset voltage and high 2V/µs slew rate make this device ideal for signal-conditioning stages for precision, low-voltage data-acquisition systems. The MAX4321 comes in a space-saving 5-pin SOT23 package and is guaranteed over the extended (-40°C to +85°C) temperature range.

Patina

The MAX4321 is a low-voltage, pin-for-pin compatible upgrade for the LMC7101 that offers five-times higher bandwidth, two-times faster slew rate, and about half the input voltage noise density.

B. Absolute Maximum Ratings

ltom

<u>item</u>	Raung
Supply Voltage (VCC to VEE) All other Pins Output Short-Circuit Duration Storage Temp. Lead Temp. (10 sec.)	-0.3V to +7V (VEE - 0.3V to (VCC + 0.3V) Continuous -65°C to +150°C +300°C
Continuous Power Dissipation (TA = +70°C)	
5-Pin SOT23	571mW
Derates above +70°C 5-Pin SOT23	7.1mW/°C

II. Manufacturing Information

A. Description: Low-Voltage, Rail-to-Rail Input/Output, SOT23 5MHz Op Amp

B. Process: CB20

C. Number of Device Transistors: 84

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia

F. Date of Initial Production: April, 2000

III. Packaging Information

A. Package Type: 5-Pin SOT23

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Non-Conductive Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-2501-0027

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 47 x 31 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Gold

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)

F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)

Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \text{ x } 4389 \text{ x } 80 \text{ x } 2} \text{ (Chi square value for MTTF upper limit)}$$

$$\text{Temperature Acceleration factor assuming an activation energy of } 0.8eV$$

$$\lambda = 13.57 \text{ x } 10^{-9}$$

$$\lambda = 13.57 \text{ F.I.T. (60% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5216) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OX42 die type has been found to have all pins able to withstand a transient pulse of ± 2500 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA and/or ± 20 V.

Table 1Reliability Evaluation Test Results

MAX4321EUK

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Tes	t (Note 1)			
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0
Moisture Testi	ng (Note 2)			
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	120	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical St	ress (Note 2)			
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

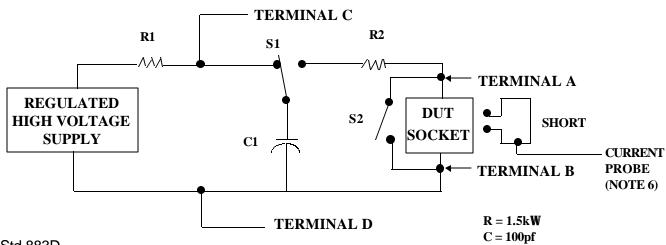
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

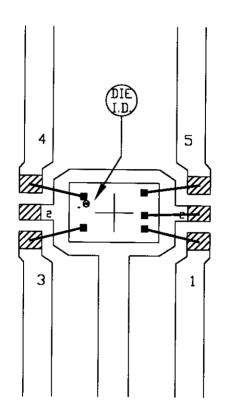
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \(\lambda_{S1} \), or \(\lambda_{S2} \) or \(\lambda_{S3} \) or \(\lambda_{CC1} \), or \(\lambda_{CC2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8

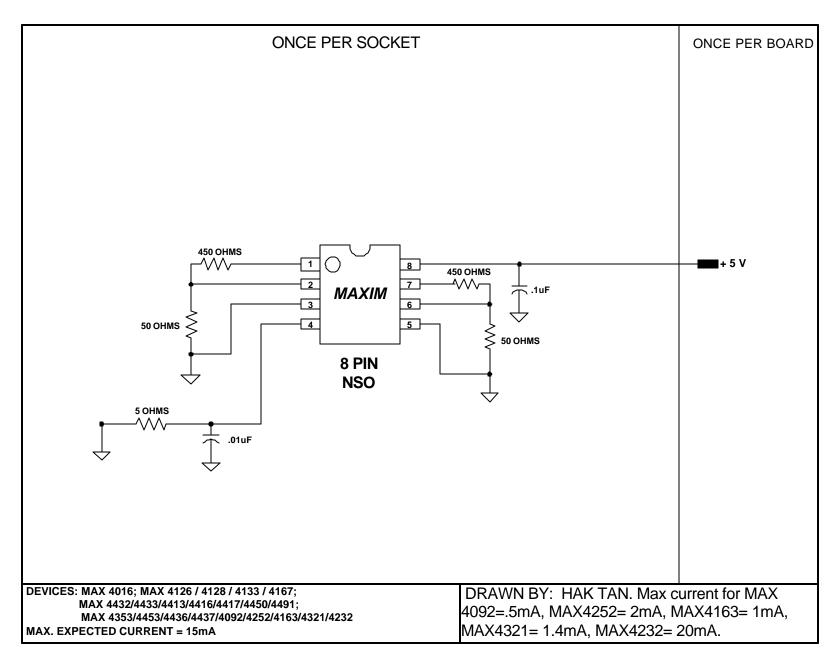


MUST USE NON-CONDUCTIVE EPOXY

Ø- BONDING AREA

NOTE: CAVITY DOWN

PKG. CODE: U5-1		SIGNATURES	DATE	CONFIDENTIAL & PROPRIE	
CAV./PAD SIZE:	PKG.			BOND DIAGRAM #:	REV:
64X45	DESIGN			05-2501-0027	Α



DOCUMENT I.D. 06-5216	REVISION I	MAXIM TITLE: BI Circuit (MAX4016/4126/4128/4133/4167/4432/4433/4413/4416/4417/4450/4491/4353/4453/443	PAGE 2 OF 3
		6/4437/4092/4252/4321/4163/4232)	