RELIABILITY REPORT

FOR

MAX4292EBL

PLASTIC ENCAPSULATED DEVICES

September 16, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX4292 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4292 micropower operational amplifier operates from a 1.8V to 5.5V single supply or ±0.9V to ±2.75V dual supplies and has Rail-to-Rail® input/output capabilities. This amplifiers provides a 500kHz gain-bandwidth product and 120dB open-loop voltage gain while using only 100µA of supply current per amplifier. The combination of low input offset voltage (±200µV) and high open-loop gain makes them ideal for low-power/low-voltage, high-precision portable applications.

The MAX4292 has an input common-mode range that extends to each supply rail, and it's outputs swing to within 46mV of the rails with a 2kΩ load. Although the minimum operating voltage is specified at 1.8V, this device typically operate down to 1.5V. The combination of ultra-low-voltage operation, rail-to-rail inputs/output, and low-power consumption makes this device ideal for any portable/two-cell battery-powered system.

The dual MAX4292 is offered in a space-saving 8-bump, 1.5mm X 1.5mm footprint, ultra chip-scale package (UCSP™).

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage (VCC to VEE)	6V
All Other Pins	(VCC + 0.3V) to (VEE - 0.3V)
Current into IN_+, IN_-	±25mA
Output Short-Circuit Duration	Continuous
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Bump Temperature (soldering) (Note 1)	
Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C
Continuous Power Dissipation	
8-Bump UCSP	379mW
Derates above +70°C	
8-Bump UCSP	4.7mW/°C

Note 1: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection Reflow. Preheating is required. Hand or wave soldering is not allowed.

II. Manufacturing Information

A. Description/Function:	Ultra-Small, 1.8V, µPower, Rail-to-Rail I/O Op Amps
B. Process:	S8 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	356
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines or USA
F. Date of Initial Production:	July, 2001

III. Packaging Information

A. Package Type:	**8-Bump UCSP**
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	# 05-2501-0161
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

IV. Die Information

A. Dimensions:	62 x 62 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$

$\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5547) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The OX82 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±150mA.

Table 1
Reliability Evaluation Test Results

MAX4292EBL

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	UCSP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		N/A	N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-40°C/125°C 1000 Cycles Slow Ramp (Note 3)	DC Parameters	UCSP	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: UCSP Temperature Cycle performed at with a ramp rate of 11°C/minute, dwell=15 minutes, one cycle/hour

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

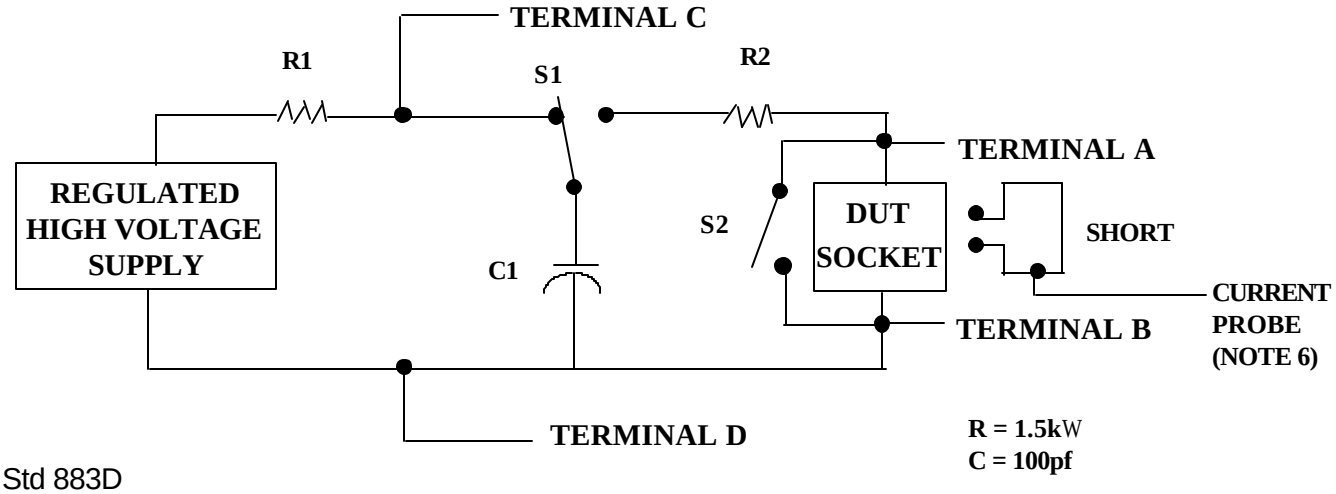
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

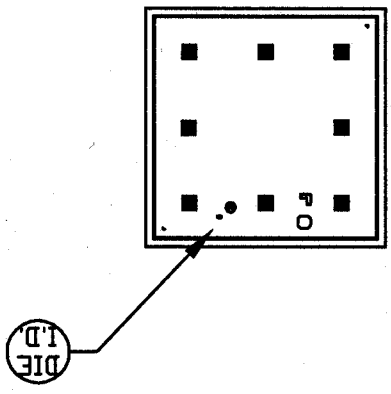
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

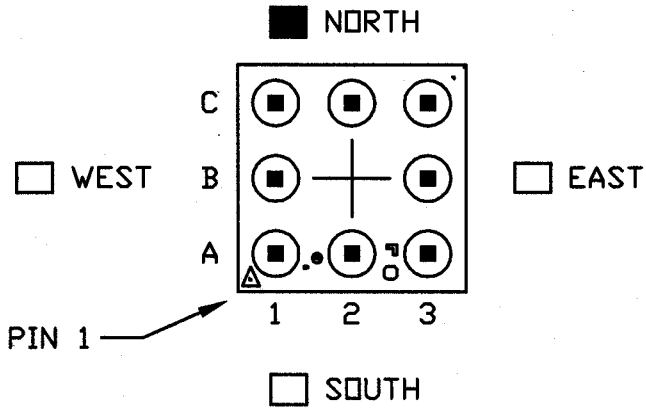


Mil Std 883D
Method 3015.7
Notice 8

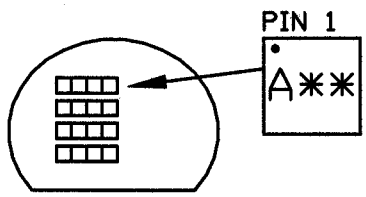
ORIGINAL CHIP



AFTER BUMP

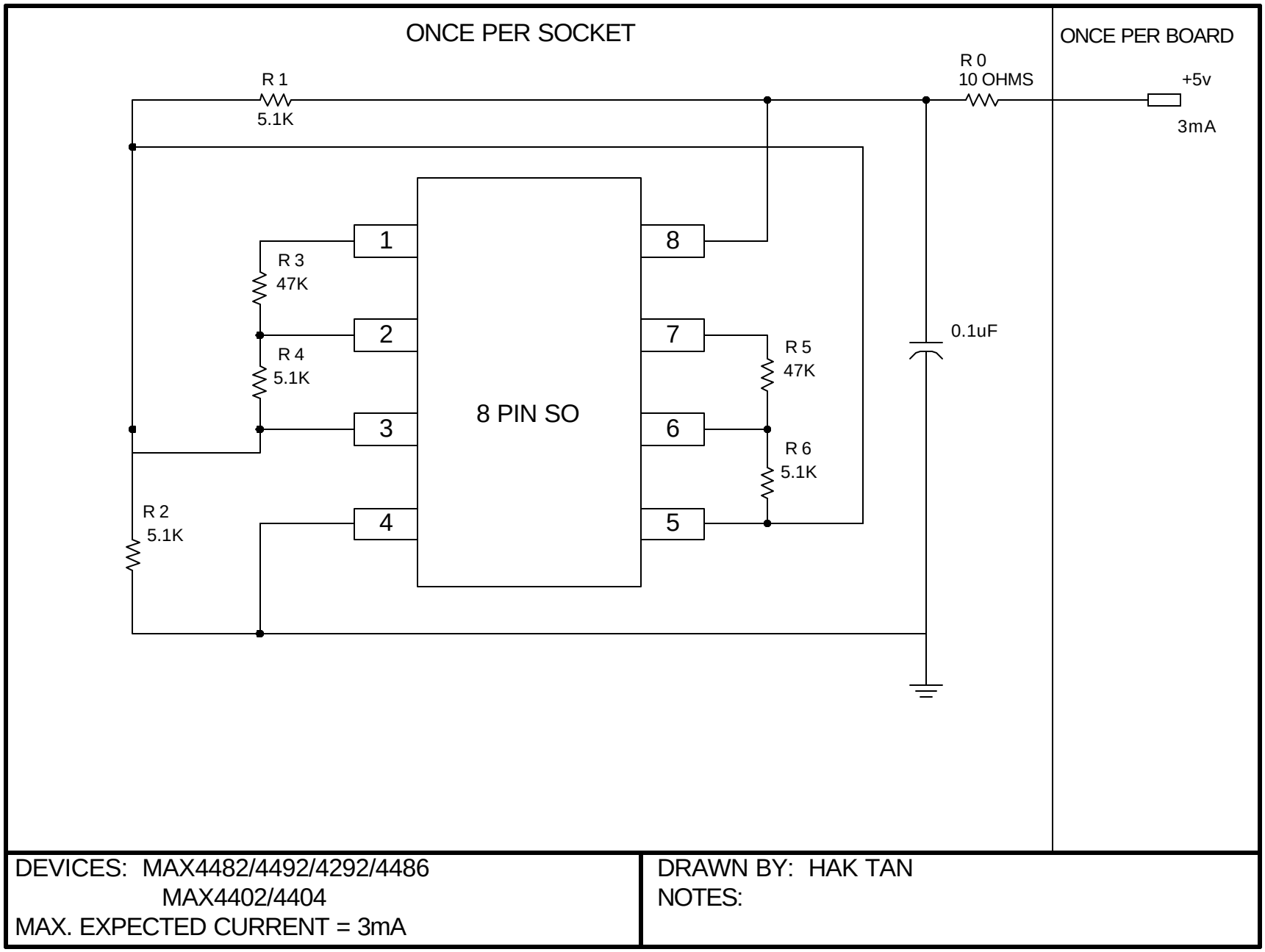


SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.



PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)

PKG. CODE: B9-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: N/A	PKG. DESIGN			BOND DIAGRAM #: 05-2501-0161	REV: A



DEVICES: MAX4482/4492/4292/4486
MAX4402/4404
MAX. EXPECTED CURRENT = 3mA

DRAWN BY: HAK TAN
NOTES: