

RELIABILITY REPORT
FOR
MAX4236xxx
PLASTIC ENCAPSULATED DEVICES

June 14, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Conclusion

The MAX4236 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4236 is a high-precision op amps that features an exceptionally low offset voltage and offset voltage temperature coefficient without using any chopper techniques. The MAX4236 has a typical large-signal, open-loop voltage gain of 120dB. These devices have an ultra-low input-bias current of 1pA. The MAX4236 is unity-gain stable with a gain-bandwidth product of 1.7MHz. This device has a shutdown function in which the quiescent current is reduced to less than 0.1µA, and the amplifier output is forced into a high-impedance state.

The input common-mode range of the MAX4236 extends below the negative supply range, and the output swings Rail-to-Rail®. These features make the amplifier ideal for applications with +3V or +5V single power supplies. The MAX4236 is specified for the extended temperature range (-40°C to +85°C) and is available in tiny SOT23, µMAX, and SO packages. For greater accuracy, the A grade µMAX and SO packages are tested to guarantee 20µV (max) offset voltage at +25°C and less than 2µV/°C drift.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Supply Voltage (VCC - VEE)	-0.3V to +6V
Analog Input Voltage (IN+ or IN-)	(VEE - 0.3V) to (VCC + 0.3V)
Logic Input Voltage (SHDN)	(VEE - 0.3V) to (VCC + 0.3V)
Current into Any Pin	20mA
Output Short-Circuit Duration	Continuous to Either VCC or VEE
Continuous Power Dissipation (TA = +70°C)	
6-Pin SOT23-6 (derate 8.7mW/°C above +70°C)	696mW
8-Pin µMAX (derate 4.5mW/°C above +70°C)	362mW
8-Pin SO (derate 5.9mW/°C above +70°C)	471mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	<i>SOT23, Very High Precision, 3V/5V Rail-To-Rail Op Amps</i>
B. Process:	B12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	224
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Dallas, Korea, Malaysia, Philippines or Thailand
F. Date of Initial Production:	July, 2001

III. Packaging Information

A. Package Type:	8-Pin μMAX	8-Pin SO	6 SOT23-6
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	100% Matte Tin	100% Matte Tin	100% Matte Tin
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-2501-0173	# 05-2501-0172	#05-2501-0174
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	33 x 57 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.73 \times 10^{-9}$$

$$\lambda = 13.73 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-5655) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.10 @ 25°C and 1.78 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The OX59Z die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX4236xExx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX	77	0
			SO	77	0
			SOT	77	
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

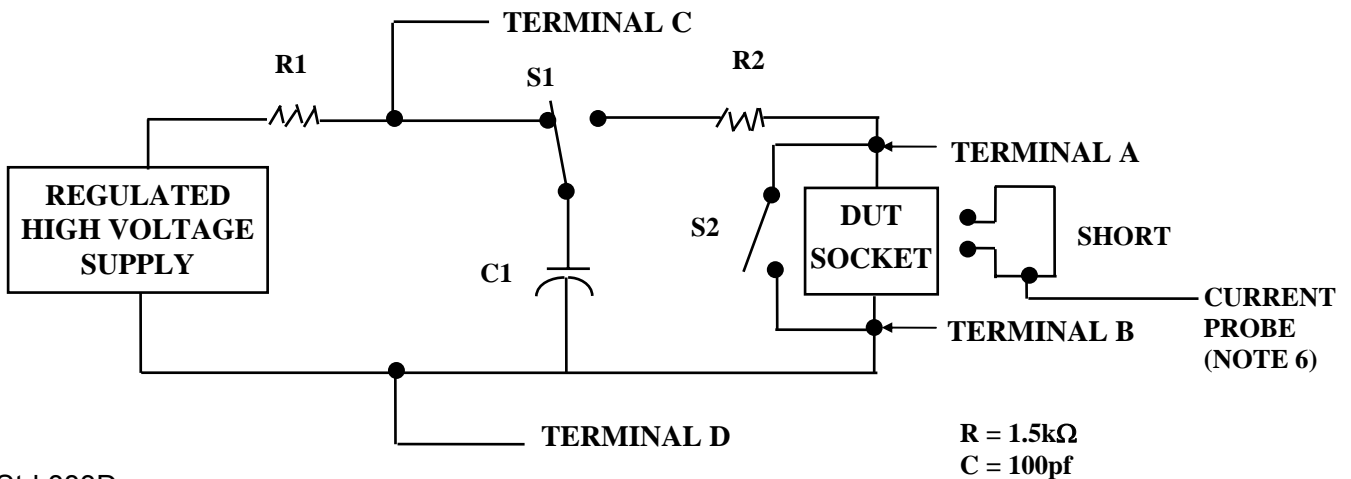
2/ No connects are not to be tested.

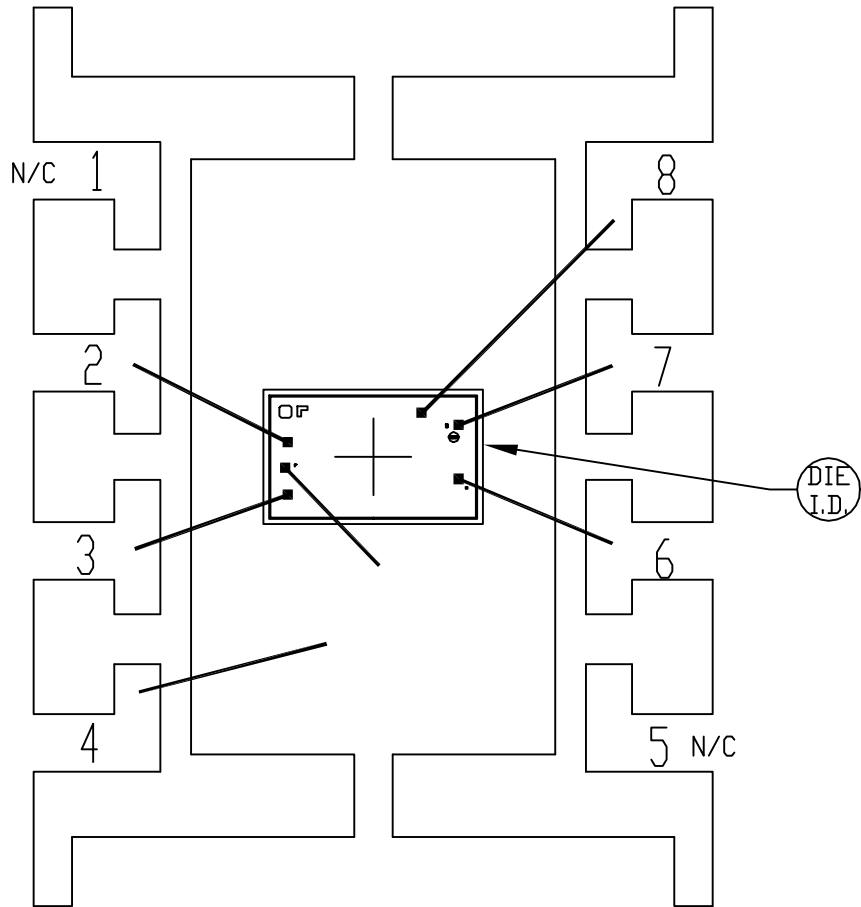
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

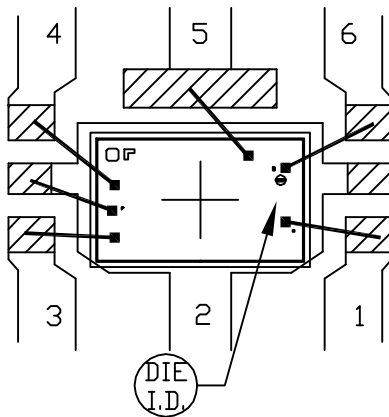
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



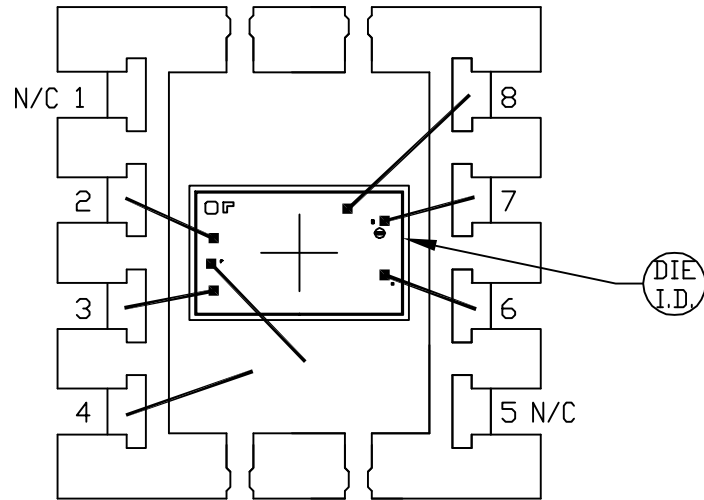


PKG. CODE: S8-5		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 95 X 155	PKG.		2/7/01	BOND DIAGRAM #:	REV:
	DESIGN		2/8/01	05-2501-0172	A

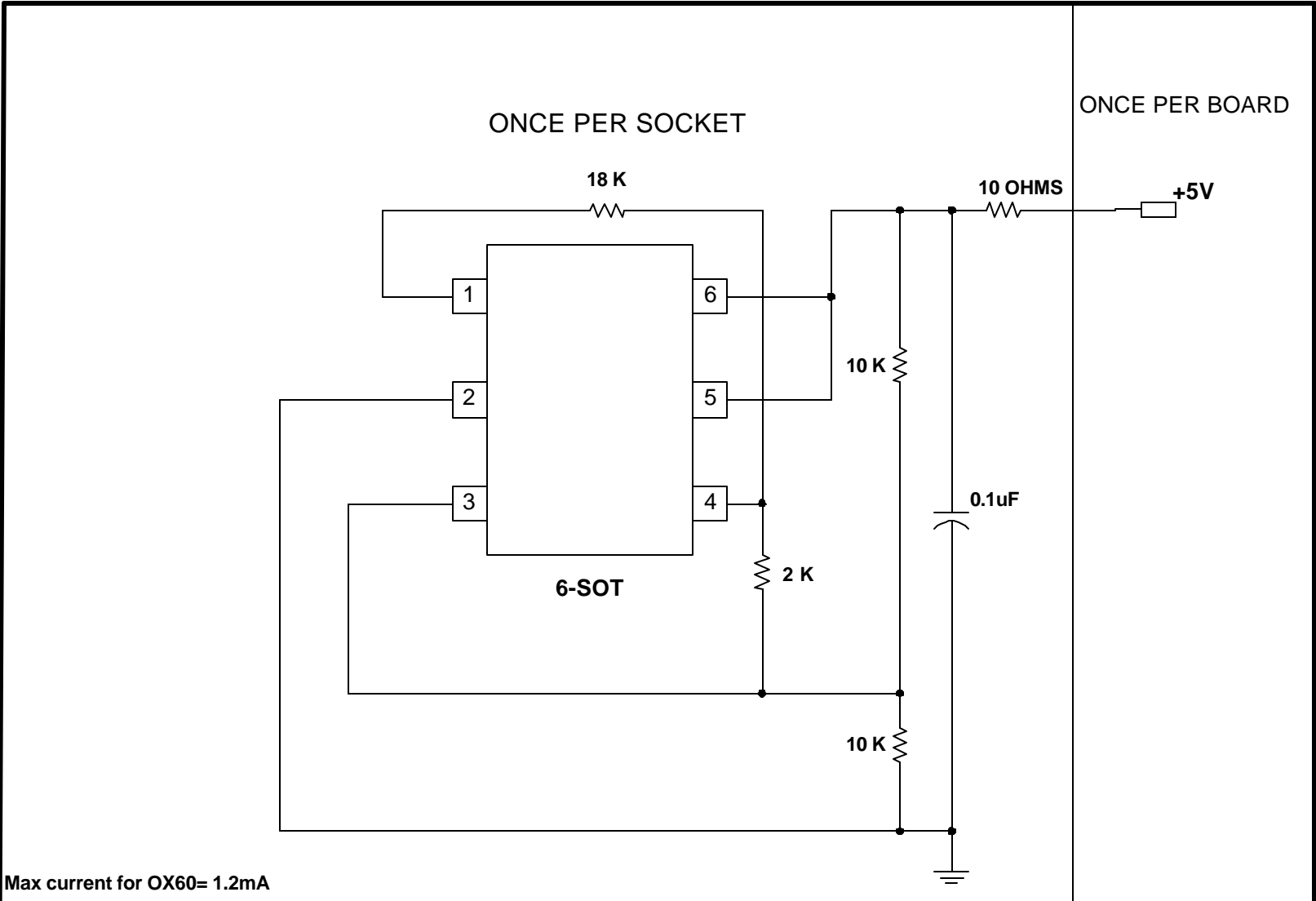


NOTE: CAVITY DOWN

PKG. CODE: U6-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 64x39	PKG. DESIGN		2/7/01 2/8/01	BOND DIAGRAM #: 05-2501-0174	REV: A



PKG. CODE: U8-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68x94	PKG. DESIGN		2/7/01 2/8/01	BOND DIAGRAM #: 05-2501-0173	REV: A



Max current for OX60= 1.2mA

Devices:MAX 4289/4236/4237/4300/4390/4389/4390E/4239
 4389E/4450E/4380E/4082/4083/4082E/4083E/4385E/4238
 Max current=10mA (400 uA for MAX4289/6mA for MAX4300)

E/4389E/4450E/4380E/4390/4389.
 Max current for Max4238/4239=1.2mA.