

RELIABILITY REPORT  
FOR  
**MAX4224Exx**  
PLASTIC ENCAPSULATED DEVICES

June 20, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord  
Quality Assurance  
Manager, Reliability Operations

Reviewed by



Bryan J. Preeshl  
Quality Assurance  
Executive Director

## Conclusion

The MAX4224 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ....Device Description	V. ....Quality Assurance Information
II. ....Manufacturing Information	VI. ....Reliability Evaluation
III. ....Packaging Information	
IV. ....Die Information	.....Attachments

### I. Device Description

#### A. General

The MAX4224 current-feedback amplifier combines ultra-high-speed performance, low distortion, and excellent video specifications with low-power operation. The MAX4224 has a shutdown feature that reduces power-supply current to 350 $\mu$ A and places the outputs into a high-impedance state. This device operates with dual supplies ranging from  $\pm 2.85$ V to  $\pm 5.5$ V and provides a typical output drive current of 80mA. The MAX4224 is compensated for a closed-loop gain of +2 (6dB) or more, and has a -3dB bandwidth of 600MHz (1.2GHz gain-bandwidth product).

The MAX4224 is ideal for professional video applications, with differential gain and phase errors of 0.01% and 0.02°, 0.1dB gain flatness of 300MHz, and a 1100V/ $\mu$ s slew rate. Total harmonic distortion (THD) of -60dBc (10MHz) and an 8ns settling time to 0.1% suit these devices for driving high-speed analog-to-digital inputs or for data-communications applications. The low-power shutdown mode on the MAX4224 makes it suitable for portable and battery-powered applications. Its high output impedance in shutdown mode is excellent for multiplexing applications.

The single MAX4224 is available in space-saving 6-pin SOT23 packages. The device is available in the extended -40°C to +85°C temperature range.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Supply Voltage (VCC to VEE)	12V
Analog Input Voltage	(VEE - 0.3V) to (VCC + 0.3V)
Analog Input Current	$\pm 25$ mA
SHDN Input Voltage	(VEE - 0.3V) to (VCC + 0.3V)
Short-Circuit Duration	
OUT to GND	Continuous
OUT to VCC or VEE	5sec
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin SO	471mW
6-Pin SOT	571mW
Derates above +70°C	
8-Pin SO	5.88mW/°C
6-Pin SOT	7.1mW/°C

## II. Manufacturing Information

A. Description/Function:	1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown
B. Process:	CB20 - Complementary Bipolar Process
C. Number of Device Transistors:	87
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia or Thailand
F. Date of Initial Production:	April, 1997

## III. Packaging Information

A. Package Type:	<b>8-Lead SO</b>	<b>6-Lead SOT23</b>
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-3001-0050	# 05-3001-0051
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

## IV. Die Information

A. Dimensions:	57 x 27 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Gold
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	iO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 240 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 4.52 \times 10^{-9} \quad \lambda = 4.52 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5130) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The OP29-1 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2500\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX4224Exx**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SO SOT23	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

## Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

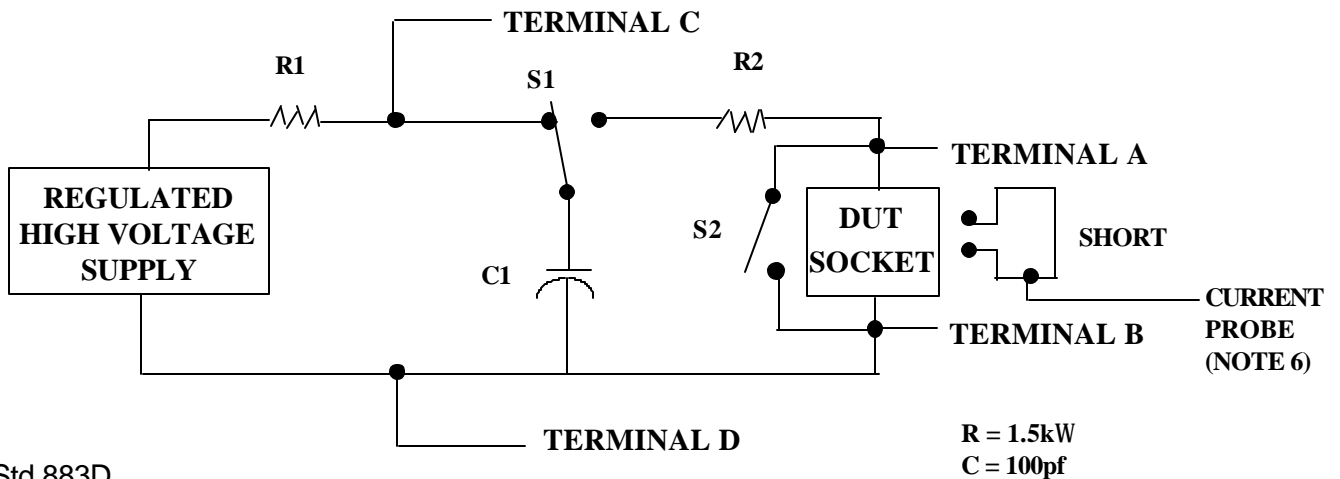
2/ No connects are not to be tested.

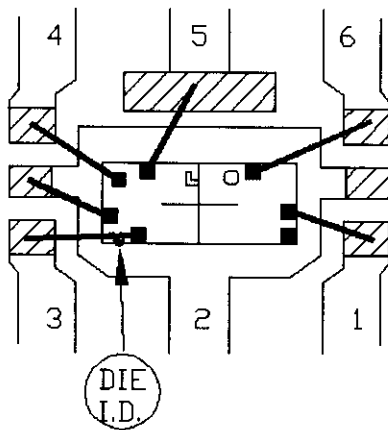
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

### 3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

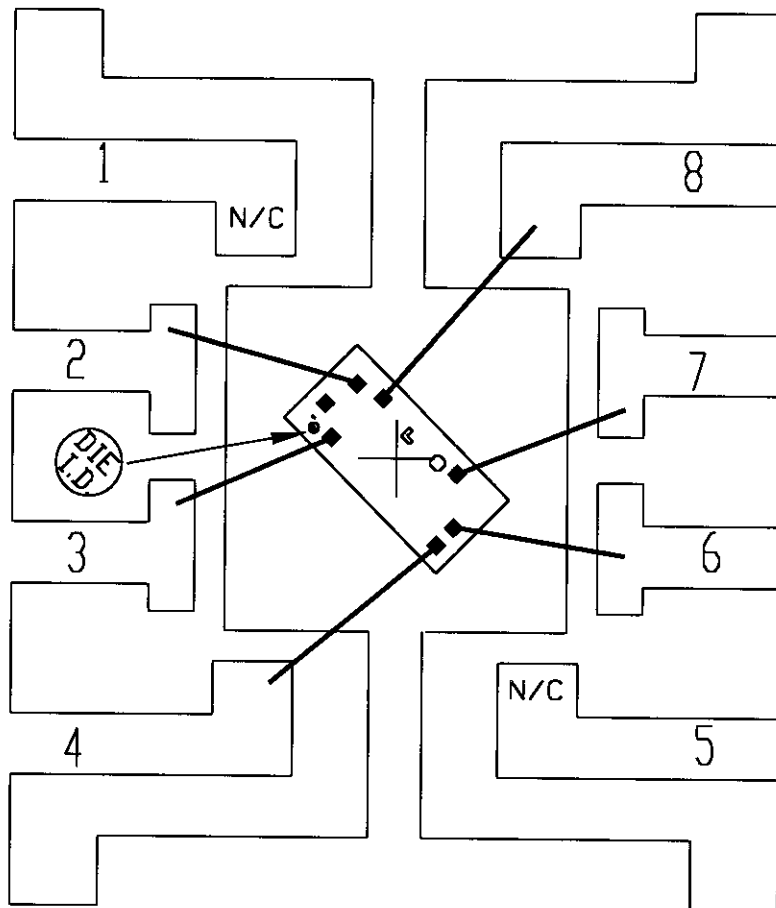




Ø - BONDING AREA

NOTE: CAVITY DOWN

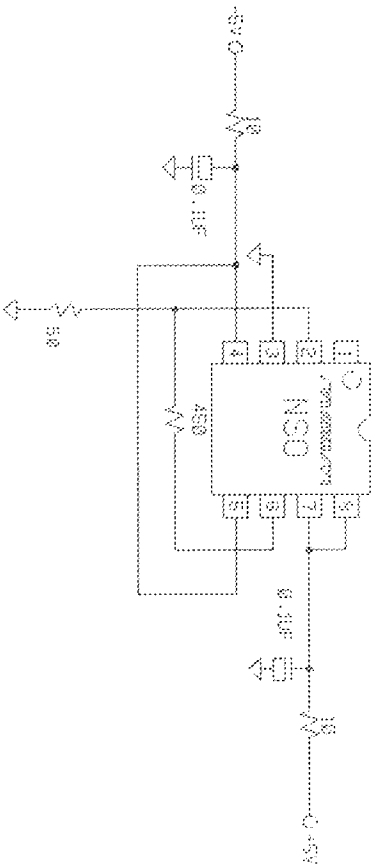
PKG.CODE: U6-1		APPROVALS	DATE	<b>MAXIM</b>	
CAV./PAD SIZE: 64X39	PKG. DESIGN			BUILDSHEET NUMBER: 05-3001-0051	REV.: A



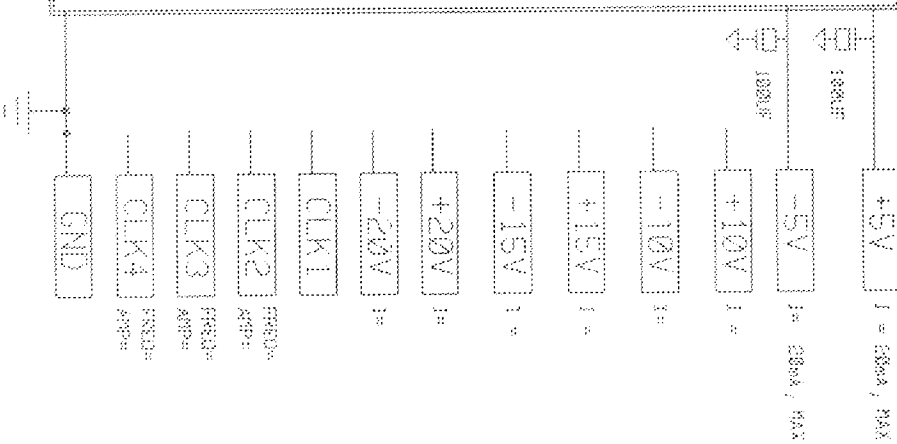
PKG. CODE: S8-2		SIGNATURES	DATE	<b>MAXIM</b> CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 90 X 90	PKG. DESIGN			BOND DIAGRAM #: 05-3001-0050	REV: A



ONCE PER SOCKET



ONCE PER BOARD



... STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1006.  
 ... BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 100 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST SHOW ISQC CONTINGENTS
4. APPROVED FOR EX COMMERCIAL INJ 40/880

SPEC. NO. 06-5130 REV. C

MAX IN BURN-IN SCHEMATIC

DATE: 8/4/95

REVISE TYPE: MAX100-4100 MAX4200/1/2  
 MAX477 MAX150/4150 MAX450/1

DRAWN BY: C. JONES

MAX100/4150 MAX450/7/6