RELIABILITY REPORT

FOR

MAX4106ESA

PLASTIC ENCAPSULATED DEVICES

August 7, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX4106 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description
II.Manufacturing Information
III.Packaging Information
IV.Die Information
IV.Die Information
IV.Die Information

I. Device Description

A. General

The MAX4106 op amp combines high-speed performance with ultra-low-noise performance. The MAX4106 is compensated for closed-loop gains of 5V/V.

The MAX4106 requires only 15mA of supply current while delivering a 350MHz bandwidth. Voltage noise is an ultra-low 0.75nV/ $\sqrt{\text{Hz}}$, while a low-distortion architecture provides a spurious-free dynamic range (SFDR) of 63dB at 5MHz.

This high-speed op amp has a wide output voltage swing of ± 3.2 V and a high current-drive capability of 80mA.

B. Absolute Maximum Ratings

<u>Item</u>	Rating	
Power-Supply Voltage (V_{CC} to V_{EE})	12V	
Voltage on Any Pin to Ground or Any Other Pin	$ m V_{CC}$ to $ m V_{EE}$	
Short-Circuit Duration (V _{OUT} to GND)	Continuous	
Storage Temp.	-65° C to $+160^{\circ}$ C	
Junction Temperature	+150°C	
Lead Temp. (10 sec.)	+300°C	
Power Dissipation		
8 Lead SO	471mW	
Derates above +70°C		
8 Lead SO	5.88mW/°C	

II. Manufacturing Information

A. Description/Function: 350MHz, Ultra-Low-Noise Op Amp

B. Process: CP10

C. Number of Device Transistors: 55

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines, Malaysia, or Thailand

F. Date of Initial Production: September, 1995

III. Packaging Information

A. Package Type: **8 Lead SO**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-0601-0449

H. Flammability Rating: Class UL94-V0

IV. Die Information

A. Dimensions: 37 x 40 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Gold

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)

F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)

Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

 $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83 \quad \text{(Chi}}{192 \text{ x } 4389 \text{ x } 80 \text{ x } 2}$$

$$\lambda = 13.57 \text{ x } 10^{-9}$$
Temperature Acceleration factor assuming an activation energy of 0.8eV

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5130) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85° C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The OA81 die type has been found to have all pins able to withstand a transient pulse of ± 2000 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 100 mA and/or ± 20 V.

Table 1Reliability Evaluation Test Results

MAX4106ESA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	(Note 1) $Ta = 135^{\circ}C$ Biased $Time = 192 \text{ hrs.}$	DC Parameters & functionality	80	0
Moisture Testin	ng (Note 2)			
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	97	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Str	ress (Note 2)			
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.

Note 2: Generic process/package data

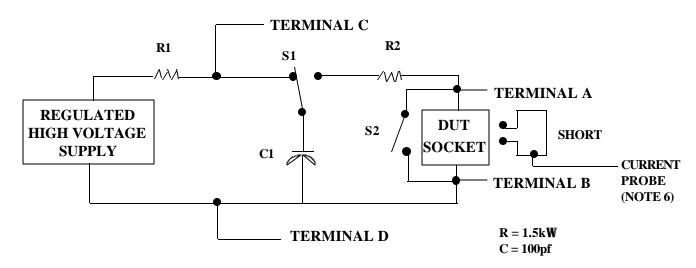
TABLE II. Pin combination to be tested. 1/2/

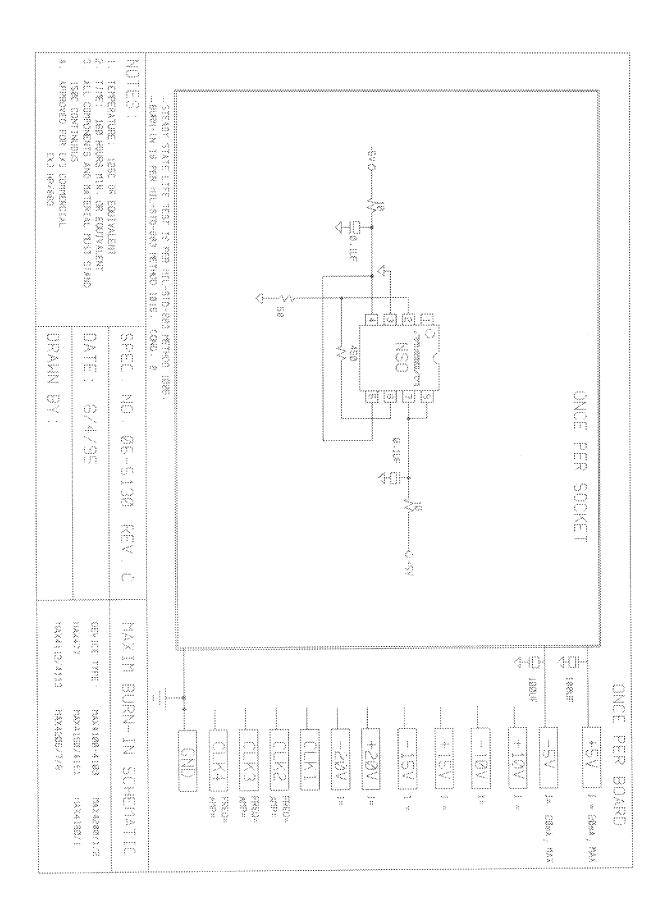
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

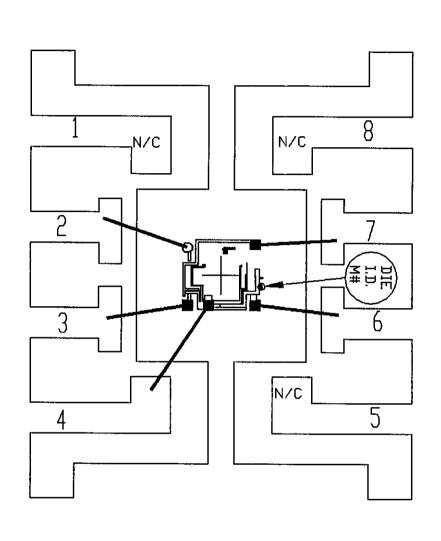
- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- 2/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, +V_S, -V_S, V_{REF}, etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.







PKG.CODE: S8-5		APPROVALS	DATE	MAXI	111
CAV./PAD SIZE:	PKG.		•	BUILDSHEET NUMBER:	REV.:
90 X 90	DESIGN			05-0601-0449	A