

RELIABILITY REPORT
FOR
MAX4017EUA+T
PLASTIC ENCAPSULATED DEVICES

February 21, 2013

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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Conclusion

The MAX4017EUA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX4014/MAX4017/MAX4019/MAX4022 are precision, closed-loop, gain of +2 (or -1) buffers featuring high slew rates, high output current drive, and low differential gain and phase errors. These single-supply devices operate from +3.15V to +11V, or from $\pm 1.575\text{V}$ to $\pm 5.5\text{V}$ dual supplies. The input voltage range extends 100mV beyond the negative supply rail and the outputs swing Rail-to-Rail. These devices require only 5.5mA of quiescent supply current while achieving a 200MHz -3dB bandwidth and a 600V/ μs slew rate. In addition, the MAX4019 has a disable feature that reduces the supply current to 400 μA . Input voltage noise for these parts is only 10nV/ Hz and input current noise is only 1.3pA/√Hz. This buffer family is ideal for low-power/low-voltage applications that require wide bandwidth, such as video, communications, and instrumentation systems. For space-sensitive applications, the MAX4014 comes in a tiny 5-pin SOT23 package.

II. Manufacturing Information

A. Description/Function: Outputs in SOT23	Low-Cost, High-Speed, Single-Supply, Gain of +2 Buffers with Rail-to-Rail
B. Process:	CB2
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Philippines, Thailand, Malaysia
F. Date of Initial Production:	October 25, 1997

III. Packaging Information

A. Package Type:	8-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-3001-0037
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	221°C/W
K. Single Layer Theta Jc:	41.9°C/W
L. Multi Layer Theta Ja:	206.3°C/W
M. Multi Layer Theta Jc:	41.9°C/W

IV. Die Information

A. Dimensions:	81 X 51 mils
B. Passivation:	Si ₃ N ₄ (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4340 \times 320 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 7.6 \times 10^{-9}$$

$$\lambda = 7.6 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the CB2 Process results in a FIT Rate of 0.06 @ 25C and 0.95 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot BC7BCQ003B D/C 9740, Latch-Up lot NC7BD9015A D/C 0032)

The OP06-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX4017EUA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C	DC Parameters	80	0	NC7ADQ001A, D/C 9916
	Biased	& functionality	80	0	BC7ACN002A, D/C 9743
	Time = 192 hrs.		80	1	NC7BD9015A, D/C 0032
				80	0

Note 1: Life Test Data may represent plastic DIP qualification lots.