RELIABILITY REPORT

FOR

MAX3964xxP

PLASTIC ENCAPSULATED DEVICES

August 14, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3964 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3964 limiting amplifier, with $2mV_{P-P}$ input sensitivity and PECL data outputs, is ideal for low-cost ATM, FDDI, and Fast Ethernet fiber optic applications.

The MAX3964 features an integrated power detector that senses the input-signal power. It provides a received-signal-strength indicator (RSSI), which is an analog indication of the power level and complementary PECL loss-of-signal (LOS) outputs, which indicate when the power level drops below a programmable threshold. The threshold can be adjusted to detect signal amplitudes as low as 2.7mVp-p. An optional squelch function disables switching of the data outputs by holding them at a known state during an LOS condition.

The MAX3964 is available in die form, as tested wafers, and in 20-pin QSOP or thin QFN packages.

B. Absolute Maximum Ratings

Item	Rating
(SUB, GND, GNDO tied to ground)	
VCC, VCCO	-0.5V to +7.0V
FILTER, RSSI, IN+, IN-, CZP, CZN, SQUELCH,	
LOS+, LOS-, INV, VTH, OUT+, OUT-	-0.5V to (VCC + 0.5V)
PECL Output Current (OUT+, OUT-, LOS+, LOS-)	50mA
Differential Voltage Between CZP and CZN	-1.5V to +1.5V
Differential Voltage Between IN+ and IN-	-1.5V to +1.5V
Continuous Power Dissipation (TA = +70°C)	
Operating Temperature Range	-40°C to +85°C
Operating Junction Temperature Range (die)	-40°C to +150°C
Processing Temperature (die)	+400°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +70°C)	
20-Pin Thin QFN	1349mW
20-Pin QSOP	500mW
Derates above +70°C	
20-Pin Thin QFN	16.9mW/°C
20-Pin QFN	6.7mW/°C

II. Manufacturing Information

A. Description/Function: +3.0V to +5.5V, 125Mbps to 266Mbps Limiting Amplifiers with Loss-of-Signal Detector

B. Process:	GST2 (High-Speed Double Poly-Silicon Bipolar Process)
C. Number of Device Transistors:	915
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea, Thailand, Philippines or Malaysia
F. Date of Initial Production:	January, 1998

III. Packaging Information

	20-Pin QFN	**20-QSOP**
A. Package Type:		
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9001-0206	# 05-7001-0296
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	57 x 47 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Poly / Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.4 microns (as drawn)
F. Minimum Metal Spacing:	1.4 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Reliability Operations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 10.11 \times 10^{-9}$ $\lambda = 10.11$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M or RR-2BA**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HF18 die type has been found to have all pins able to withstand a transient pulse of <200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA.

Table 1
Reliability Evaluation Test Results

MAX3964xxP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN QSOP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

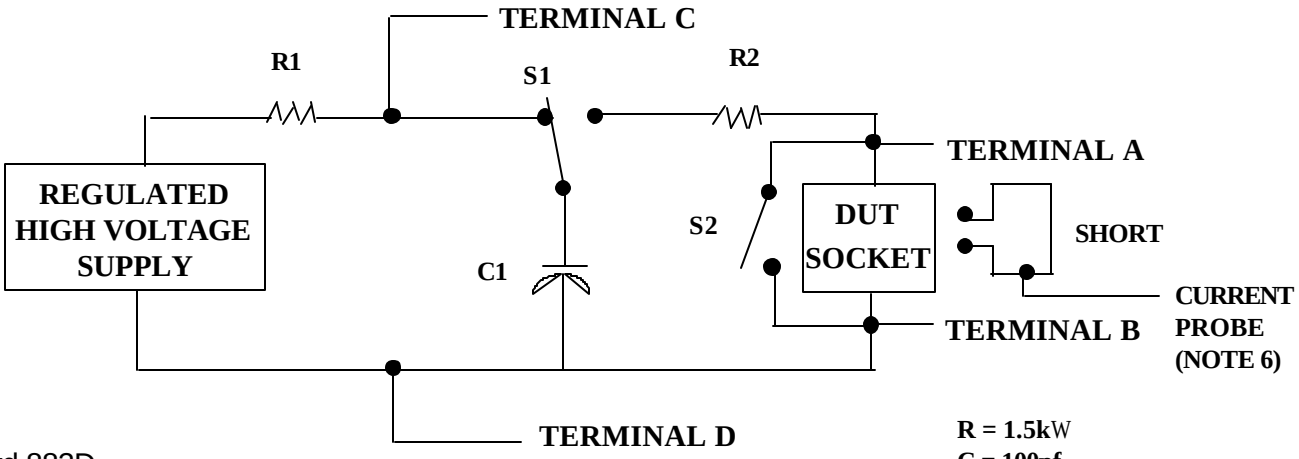
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

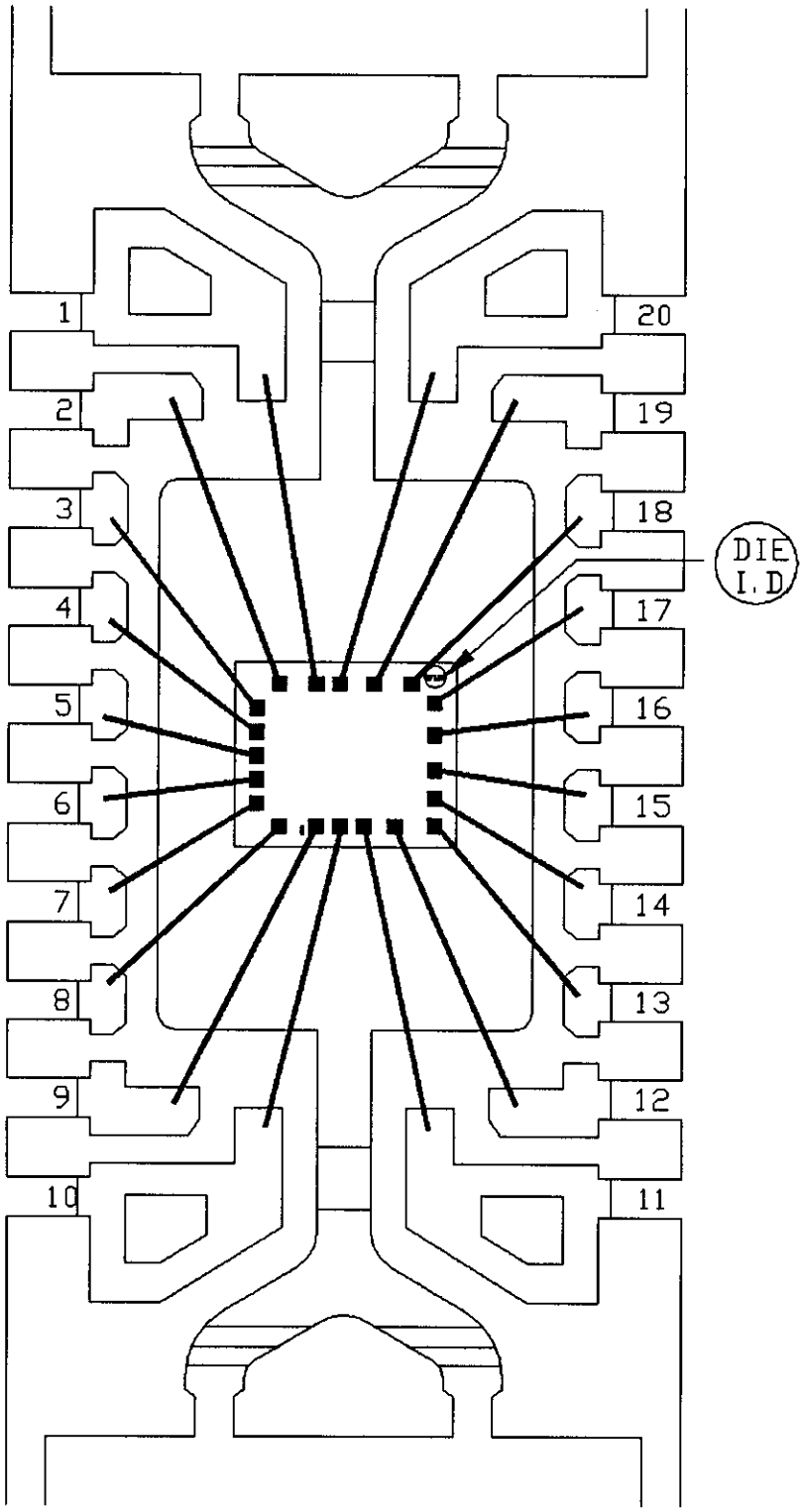
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

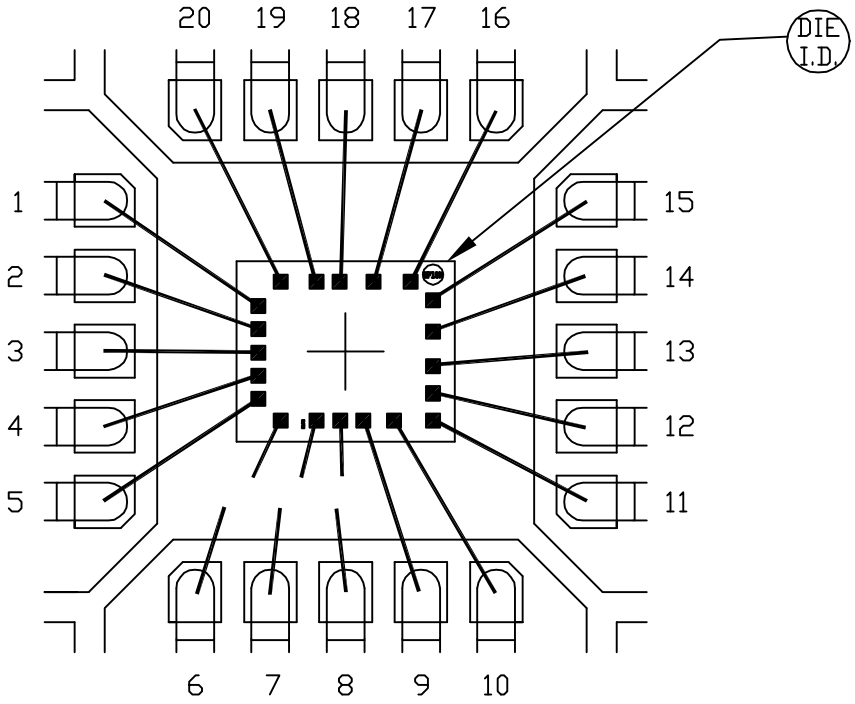


Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: E20-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 96X140	PKG. DESIGN			BUILDSHEET NUMBER: 05-7001-0296 / REV.: A

4x4x0.80mm QFN THIN PKG. EXPOSED PAD PKG.



PKG. CODE: T2044-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 98x98	PKG.			BOND DIAGRAM #: 05-9000-0206	REV: A
	DESIGN				