RELIABILITY REPORT

FOR

MAX394EUP+T

PLASTIC ENCAPSULATED DEVICES

November 29, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX394EUP+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. .....Device Description
II. .....Manufacturing Information
III. .....Packaging Information
.....Attachments
IV. .....Die Information
V. .....Quality Assurance Information
VI. .....Reliability Evaluation

I. Device Description

A. General

The MAX394 is a precision, low-voltage, quad, single-pole/double-throw (SPDT) analog switch. The four independent switches operate with bipolar supplies ranging from ±2.7V to ±8V, or with a single supply of +2.7V to +15V. The MAX394 offers low on-resistance (less than 35), guaranteed to match within 2 between channels and to remain flat over the analog signal range (4 max). It also offers break-before-make switching (10ns typical), with turn-off times less than 75ns and turn-on times less than 130ns. The MAX394 is ideal for portable operation since quiescent current runs less than 1µA with all inputs high or low. This monolithic, quad switch is fabricated with Maxim's low voltage silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption (10µW), and electrostatic discharge (ESD) greater than 2000V. Logic inputs are TTL and CMOS compatible and guaranteed over a +0.8V to +2.4V range for supply voltages up to +8V. When supplies exceed +8V, the inputs are typically +0.8V to +4V. Logic inputs and switched analog signals can range anywhere between the supply voltages without damage.

II. Manufacturing Information

A. Description/Function:	Low-Voltage, Quad, SPDT, CMOS Analog Switch-Replaces MAX333A
B. Process:	SG5
C. Fabrication Location:	USA
D. Assembly Location:	Philippines, Thailand
E. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	20-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1795
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	91°C/W
K. Single Layer Theta Jc:	20°C/W
L. Multi Layer Theta Ja:	73.8°C/W
M. Multi Layer Theta Jc:	20°C/W

IV. Die Information

A. Dimensions:	100X128 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the SG5 Process results in a FIT Rate of 0.12 @ 25C and 2.04 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AG72 die type has been found to have all pins able to withstand an HBM transient pulse of +/-3000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX394EUP+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.