RELIABILITY REPORT

FOR

MAX3831UCB-D

PLASTIC ENCAPSULATED DEVICES

October 25, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Don Lipps
Quality Assurance
Manager, Reliability Engineering

Conclusion

The MAX3831UCB-D successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX3831/MAX3832 are 4:1 multiplexers (muxes) and 1:4 demultiplexers (demuxes) with automatic channel alignment. Operating from a single +3.3V supply, the mux receives four parallel, 622Mbps SDH/SONET channels. These channels are bit interleaved to generate a serial data stream of 2.488Gbps for interfacing to an optical or an electrical driver. A 10-bit-wide elastic buffer tolerates up to ±7.5ns skew between any parallel data input and the reference clock. An external 155MHz reference clock is required for the on-chip PLL to synthesize a high-frequency 2.488GHz clock for timing the outgoing data streams. The MAX3831/MAX3832's demux receives 2.488Gbps serial data and the 2.488GHz clock from an external clock/data recovery device (MAX3876), converting it to four 622Mbps LVDS outputs. The MAX3831 provides a 622MHz LVDS clock output, and the MAX3832 provides a 155MHz LVDS clock output. An internal frame detector looks for a 622Mbps SDH/SONET framing pattern and rolls the demux to maintain proper channel assignment at the outputs. These devices also include an embedded pattern generator that enables a full-speed, built-in self-test (BIST). Two different loopback modes provide system test flexibility. A TTL loss-of-frame monitor is included. The MAX3831/MAX3832 are available in 64-pin TQFP-EP (exposed paddle) packages and are specified over the upper commercial (0°C to +85°C) temperature range.

II. Manufacturing Information

A. Description/Function:	+3.3V, 2.5Gbps, SDH/SONET, 4-Channel Interconnect Mux/Demux ICs with Clock Generator
B. Process:	GST2
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Korea
F. Date of Initial Production:	October 22, 1999

III. Packaging Information

A. Package Type:	64-pin TQFP
B. Lead Frame:	Copper
C. Lead Finish:	85Sn/15Pb plate
D. Die Attach:	Conductive
E. Bondwire:	Au (1.2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-7001-0405
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	2°C/W

IV. Die Information

A. Dimensions:	137 X 157 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the GST2 Process results in a FIT Rate of 0.06 @ 25C and 1.10 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The HF63-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX3831UCB-D

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0

Note 1: Life Test Data may represent plastic DIP qualification lots.