MAX3822UCM
Rev. A

RELIABILITY REPORT

FOR

MAX3822UCM

PLASTIC ENCAPSULATED DEVICES

October 4, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX3822 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3822 quad limiting amplifier is ideal for multichannel systems with data rates up to 2.5Gbps. The MAX3822 operates from a single +3.3V supply, over temperatures ranging from 0°C to +85°C. A channel-select (CS) pin is provided to program single-, dual-, or quad-channel operation. The disabled channels are shut down to reduce power consumption. The output interface for all four channels is CML.

The input can be driven from 20mVp-p to 1000mVp-p differentially. The threshold voltage control is common for all four channels and is programmable by an external resistor. Four separate power detectors are incorporated to monitor the received signal level for each channel. Individual TTL-compatible loss-of-power (LOP) indicators assert low if the channel signal input is below the programmed threshold. Typically 4dB LOP-bar hysteresis (2dB optical) is provided to prevent chattering when the input signal level is close to the threshold. A general LOP-bar indicator is also provided which asserts low if one or more of the four inputs is in the LOP condition.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage (VCC)	-0.5V to +6.0V
Differential Input Voltage Swing (IN1+ - IN1-), (IN2+ - IN2-), (IN3+ - IN3-), (IN4+ - IN4-)	2Vp-p
Voltage at LOP1 , LOP2 , LOP3 , LOP4 , LOP , CS	-0.5V to (VCC + 0.5V)
Voltage at IN1+, IN1-, IN2+, IN2-, IN3+, IN3-, IN4+, IN4-	(VCC - 1V) to (VCC + 0.5V)
Voltage at VTH	+0.5V to +2.3V
Voltage at CZ1+, CZ1-, CZ2+, CZ2-, CZ3+, CZ3-, CZ4+, CZ4-	-0.5V to (VCC + 0.5V)
Current into OUT1+, OUT1-, OUT2+, OUT2-, OUT3+, OUT3-, OUT4+, OUT4-,	±22mA
Storage Temperature Range	-55°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Power Dissipation (TA = +85°C)	
48-Pin TQFP-EP	2.35W
Derates above +85°C	
48-Pin TQFP-EP	29.4mW/°C

II. Manufacturing Information

A. Description/Function: +3.3V, 2.5Gbps Quad Limiting Amplifier

B. Process: GST2 (High-Speed Double Poly-Silicon Bipolar Process)

C. Number of Device Transistors: 813

D. Fabrication Location: Oregon, USA

E. Assembly Location: Korea

F. Date of Initial Production: August, 2000

III. Packaging Information

A. Package Type: **48 Lead TQFP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.2 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-7001-0459

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity
per JEDEC standard JESD22-A112: Level 3

IV. Die Information

A. Dimensions: 90 x 102 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Poly / Au

D. Backside Metallization: None

E. Minimum Metal Width: 1.4 microns (as drawn)

F. Minimum Metal Spacing: 1.4 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliability Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 45 \times 2} \text{(Chi square value for MTTF upper limit)}$$

→ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 10.78 \times 10^{-9}$ λ= 10.78 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (#06-6953) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HF65 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V

Table 1
Reliability Evaluation Test Results

MAX3822UCM

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs. Junction Temperature = 150°C	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the TQFP package.
Note 2: Generic Package/Process Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

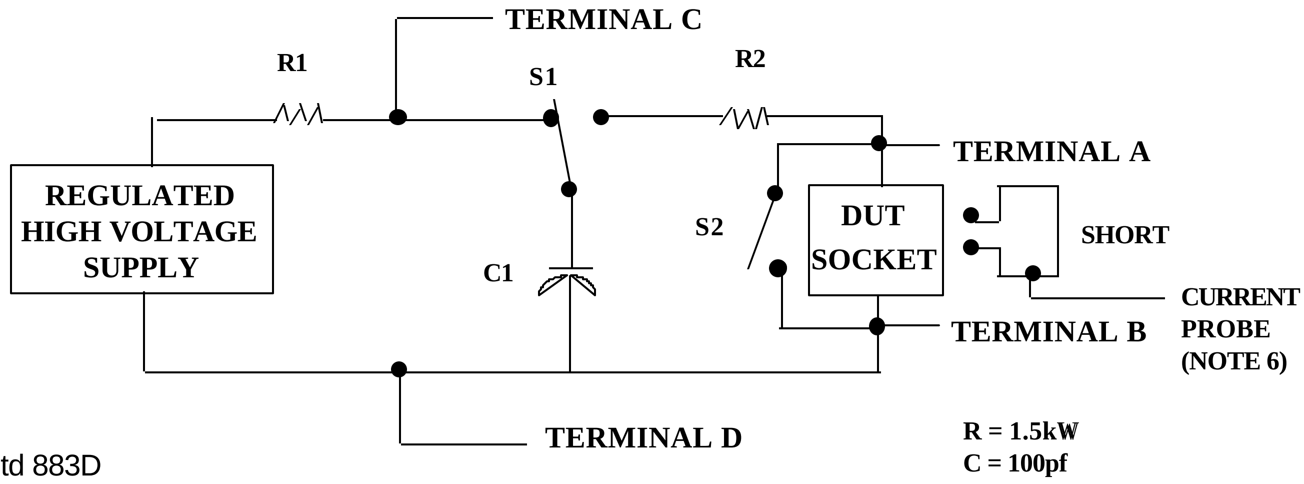
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S,}$ $-V_{S}$, V_{REF}, etc).

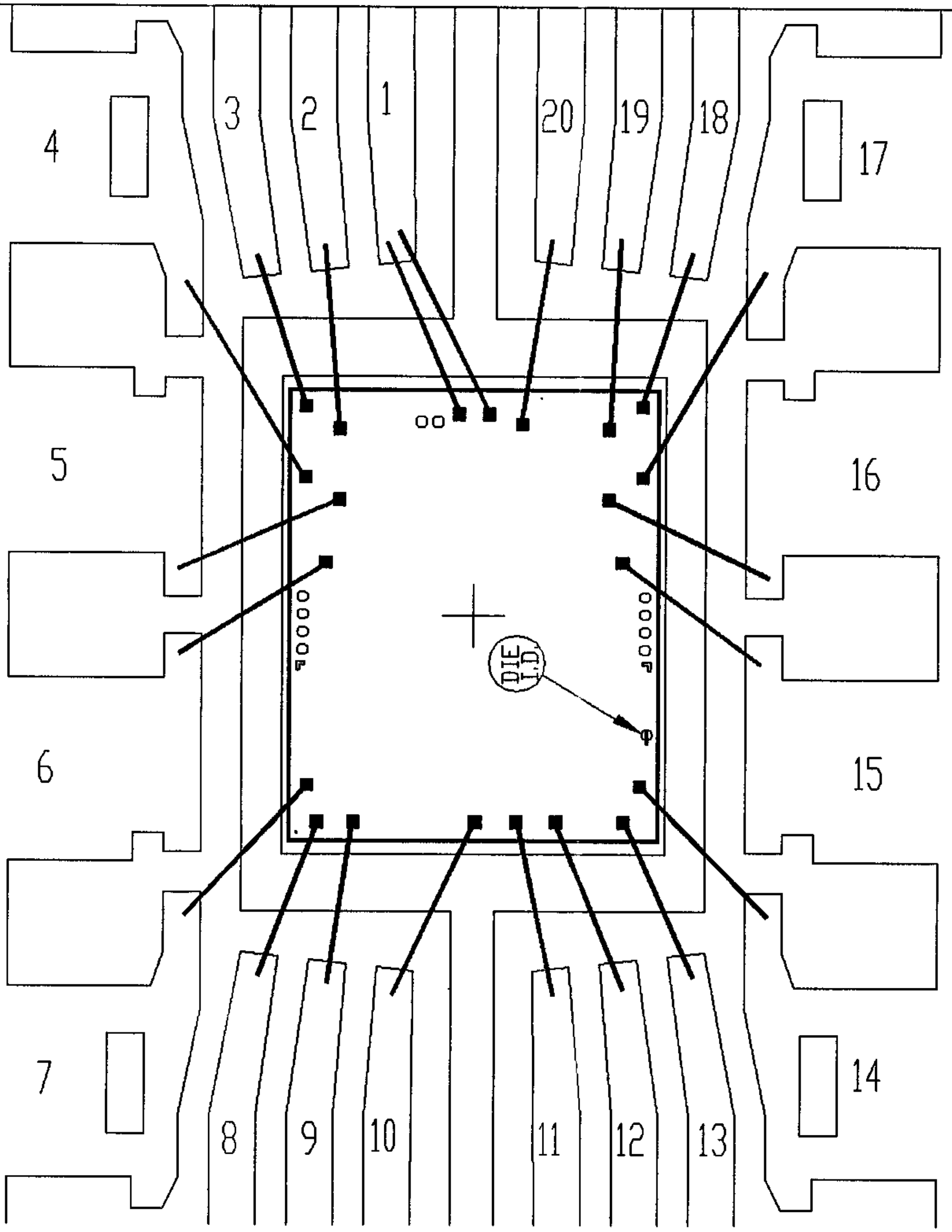
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: P20-3		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 150 X 190	PKG. DESIGN			BUILDSHEET NUMBER: 05-0401-0459
				REV.: A