



RELIABILITY REPORT
FOR
MAX3815ACCM+
PLASTIC ENCAPSULATED DEVICES

December 15, 2009

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX3815ACCM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3815A cable equalizer automatically provides compensation for DVI(tm) and HDMI(tm) v1.3 cables. It extends the usable cable distance up to 40 meters (1.65Gbps) and 35 meters (2.25Gbps). The MAX3815A is designed to equalize signals encoded in the transition-minimized differential signaling (TMDS®) format. The MAX3815A features four CML-differential inputs and outputs (three data and one clock). It provides a loss-of-signal (LOS) output that indicates loss-of-clock signal. The outputs include a disable function. Upon LOS, the chip is powered down. For direct chip-to-chip communication, the output drivers can be switched to one-half the DVI output specification to conserve power and reduce EMI. The output drive current can also be increased to allow the use of back termination resistors for improved signal integrity. Equalization can be automatic or set to manual control for specific in-cable applications. The MAX3815A is available in a 7mm x 7mm, 48-pin TQFP-EP package and operates over a 0°C to +70°C temperature range.

II. Manufacturing Information

A. Description/Function:	TMSD Digital Video Equalizer for HDMI/DVI Cables
B. Process:	G4
C. Number of Device Transistors:	9867
D. Fabrication Location:	Oregon
E. Assembly Location:	Korea
F. Date of Initial Production:	08/18/2009

III. Packaging Information

A. Package Type:	48-pin TQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3288
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Multi Layer Theta Ja:	27.6°C/W
K. Multi Layer Theta Jc:	2°C/W

IV. Die Information

A. Dimensions:	148.43X151.58 mils
B. Passivation:	Si ₃ N ₄
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9956 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 9956 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 9.99 \times 10^{-9}$$
$$\lambda = 9.99 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the G4 Process results in a FIT Rate of 0.02 @ 25C and 0.37 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HT73 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

Table 1
Reliability Evaluation Test Results

MAX3815ACCM+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data