RELIABILITY REPORT FOR

MAX3747AEUB+T / MAX3747BEUB+T

PLASTIC ENCAPSULATED DEVICES

January 17, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX3747AEUB+T / MAX3747BEUB+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3747/MAX3747A/MAX3747B multirate limiting amplifiers function as data quantizers for OC-3 through OC-48 synchronous optical network (SONET), Fibre-Channel, and Gigabit Ethernet optical receivers. They are pin-for-pin compatible with the SY88993V from Micrel Semiconductor, Inc. The amplifiers accept a wide range of input voltages and provide constant-level, current-mode logic (CML) output voltages with controlled edge speeds. The MAX3747 output voltage level is 500mVP-P and the MAX3747A/MAX3747B output voltages are 800mVP-P. The MAX3747B has enhanced LOS operation under overload conditions. The MAX3747/MAX3747A/MAX3747B limiting amplifiers feature a programmable loss-of-signal detect (LOS) and an optional disable function (DISABLE) that can be combined to implement squelch. The MAX3747/MAX3747A/MAX3747B are available in a 3mm, 10-pin µMAX® package ideal for small form-factor receivers.

II. Manufacturing Information

A. Description/Function:	155Mbps to 3.2Gbps, Low-Power SFP Limiting Amplifiers
B. Process:	CB53
C. Number of Device Transistors:	2645
D. Fabrication Location:	USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	October 25, 2007

III. Packaging Information

A. Package Type:	10-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	NiPdAu
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4252
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	180°C/W
K. Single Layer Theta Jc:	42°C/W
L. Multi Layer Theta Ja:	113.1°C/W
M. Multi Layer Theta Jc:	42°C/W

IV. Die Information

A. Dimensions:	70.86 X 77.16 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.6 / Metal2 = 0.6 / Metal3 = 1.2 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.4 / Metal2 = 0.4 / Metal3 = 1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 232 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 8.4 \times 10^{-9}$

λ = 8.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the CB53 Process results in a FIT Rate of 0.46 @ 25C and 7.85 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot JHDZEQ002B, D/C 1107)

The HT71 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX3747AEUB+T / MAX3747BEUB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Tj ~ 150C	DC Parameters	153	0	JHDZDQ001A, D/C 1038
	Biased	& functionality	79	0	JHDZDQ001E, D/C 1040
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.