

RELIABILITY REPORT  
FOR  
**MAX3665EUA**  
PLASTIC ENCAPSULATED DEVICES

March 30, 2002

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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## Conclusion

The MAX3665 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX3665 low-power transimpedance preamplifier for 622Mbps SDH/SONET applications consumes only 70mW at  $V_{CC} = 3.3V$ . Operating from a single +3.3V or +5.0V supply, it converts a small photodiode current to a measurable differential voltage. A DC cancellation circuit provides a true differential output swing over a wide range of input current levels, thus reducing pulse-width distortion. The differential outputs are back-terminated with 50 ohms per side.

The overall transimpedance gain is nominally 8kilohms. For input signal levels beyond approximately 50 $\mu$ A<sub>p-p</sub>, the amplifier will limit the output swing to 250mV. The MAX3665's low 55nA input noise provides a typical sensitivity of -33.2dBm in 1300nm, 622Mbps receivers.

The MAX3665 is designed to be used in conjunction with the MAX3676 clock recovery and data retiming IC with limiting amplifier. Together they form a complete 3.3V or 5.0V 622Mbps SDH/SONET receiver.

In die form, the MAX3665 is designed to fit on a header with a PIN diode. It includes a filter connection that provides positive bias for the photodiode through a 1.5kilohm resistor to  $V_{CC}$ . The device is available in an 8-pin  $\mu$ MAX package.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Supply Voltage ( $V_{CC}$ to GND)	-0.5V to +6V
Continuous Current at IN	+/-5mA
Voltage at OUT+, OUT-	( $V_{CC} - 1.5V$ ) to ( $V_{CC} + 0.5V$ )
Voltage at FILT	-0.5V to ( $V_{CC} + 0.5V$ )
Storage Temp.	-55°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation ( $T_A = +85^\circ C$ )	
8-Pin $\mu$ MAX	295mW
Derates above +85°C	
8-Pin $\mu$ MAX	4.5mW/°C

## II. Manufacturing Information

- A. Description/Function: 622Mbps, Ultra Low Power, 3.3V Transimpedance Preamp for SDH/SONET
- B. Process: GST3
- C. Number of Device Transistors: 2028
- D. Fabrication Location: Oregon, USA
- E. Assembly Location: Malaysia or Philippines
- F. Date of Initial Production: January, 2000

## III. Packaging Information

- A. Package Type: **8-Lead uMAX**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Silver-filled epoxy
- E. Bondwire: Gold (1.3 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: Buildsheet # 05-7001-0359
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

## IV. Die Information

- A. Dimensions: 31 x 51 mils
- B. Passivation:  $\text{Si}_3\text{N}_4/\text{SiO}_2$  (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Au
- D. Backside Metallization: None
- E. Minimum Metal Width: Metal1: 1.2; Metal2: 1.2; Metal3: 2.8; Metal4: 5.6 microns (as drawn)
- F. Minimum Metal Spacing: Metal1: 1.3; Metal2: 1.2; Metal3: 2.6; Metal4: 2.6 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric:  $\text{SiO}_2$
- I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 10.78 \times 10^{-8} \quad \lambda = 10.78 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The HF51 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 200\text{mA}$  and/or  $\pm 20\text{V}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX3665EUA**

<b>TEST ITEM</b>	<b>TEST CONDITION</b>	<b>FAILURE IDENTIFICATION</b>	<b>SAMPLE SIZE</b>	<b>NUMBER OF FAILURES</b>
<b>Static Life Test</b> (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
<b>Moisture Testing</b> (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic process/package data.

## Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

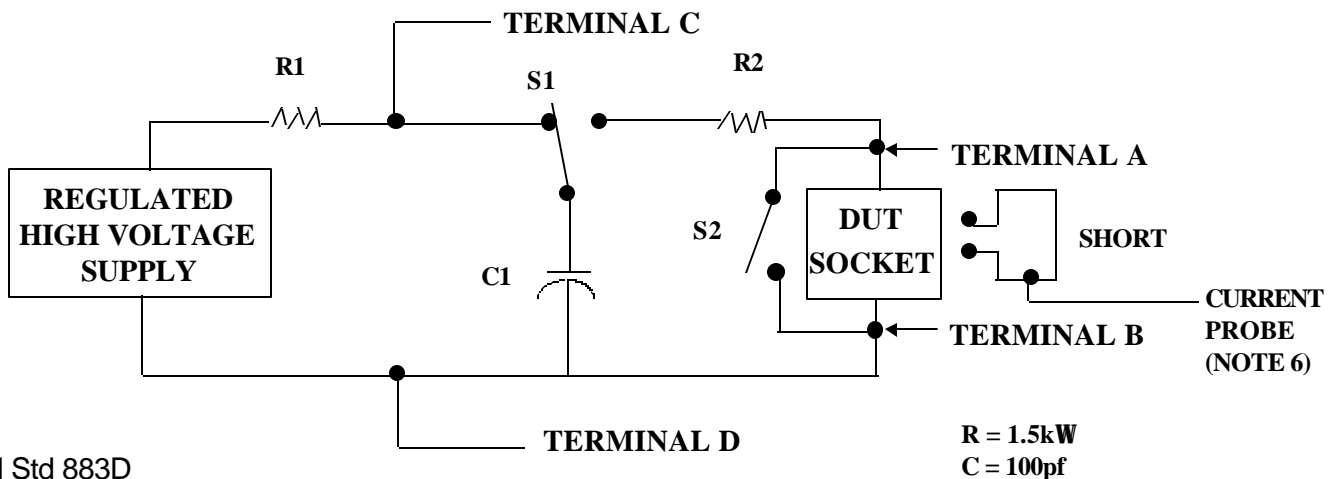
2/ No connects are not to be tested.

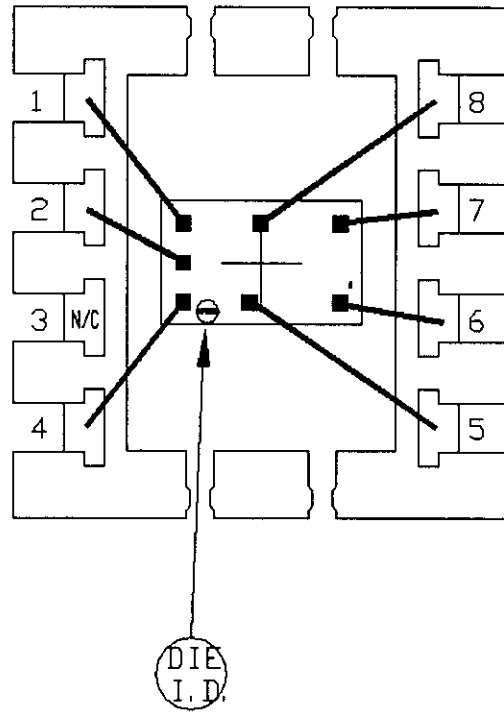
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

### 3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: U8-1

CAV./PAD SIZE:  
68X94

PKG.  
DESIGN

APPROVALS

DATE

**MAXIM**

BUILDSHEET NUMBER: 05-7001-0359  
REV.: A