RELIABILITY REPORT

FOR MAX3634ETM+

PLASTIC ENCAPSULATED DEVICES

August 11, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Richard Aburano
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX3634ETM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3634 burst-mode clock phase aligner (CPA) is designed specifically for 622Mbps or 1244Mbps GPON (ITU G.984) optical line terminal (OLT) receiver applications. The MAX3634 provides clock and clock-aligned resynchronized upstream data through differential LVPECL outputs. Using the OLT system clock as a reference, the MAX3634 aligns to the input data and acquires within the first 13 bits of the burst. The CPA operates with received data that is frequency locked to the OLT reference. The acquisition time, bit-error ratio, and jitter tolerance all support GPON PMD specifications. LVPECL high-speed clock and data outputs provide compatibility with FPGAs at 622Mbps and with the MAX3885 deserializer at 1244Mbps. The MAX3634 is available in a low-profile, 7mm x 7mm, 48-lead TQFN package. The MAX3634 operates from a single +3.3V supply, over the -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	622Mbps/1244Mbps Burst-Mode Clock Phase Aligner for GPON OLT Applications
B. Process:	G4
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	September 20, 2005

III. Packaging Information

A. Package Type:	48-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2264
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	36°C/W
K. Single Layer Theta Jc:	1.0°C/W
L. Multi Layer Theta Ja:	25°C/W
M. Multi Layer Theta Jc:	1.0°C/W

IV. Die Information

A. Dimensions:	128 x 131 mils
B. Passivation:	Si_3N_4
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Operations) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 50 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 21.9 \times 10^{-9}$

$\lambda = 21.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the G4 Process results in a FIT Rate of 0.02 @ 25C and 0.37 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NRP0CQ001B, D/C 0526)

The HT46 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 1000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/- 250mA.

Table 1
Reliability Evaluation Test Results

MAX3634ETM+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	50	0	NRP0CQ001B, D/C 0526

Note 1: Life Test Data may represent plastic DIP qualification lots.