

RELIABILITY REPORT  
FOR  
**MAX358xxE**  
PLASTIC ENCAPSULATED DEVICES

June 5, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

A handwritten signature in black ink, appearing to read 'J Pedicord'.

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Quality Assurance  
Reliability Lab Manager

Reviewed by

A handwritten signature in black ink, appearing to read 'Bryan J. Preeshl'.

Bryan J. Preeshl  
Quality Assurance  
Executive Director

## Conclusion

The MAX358 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX358 is an 8 channel single-ended (1 of 8) multiplexer with fault protection. Using a series N-channel, P-channel, N-channel structure, this multiplexer provides significantly improved fault protection. If the power supply to the MAX358 is inadvertently turned off while input voltage is still applied, all channels in the multiplexer are turned off, and only a few nanoamperes of leakage current will flow into the input. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the MAX358.

The Maxim series N-channel, P-channel, N-channel protection structure has two significant advantages. First the Maxim protection scheme limits fault currents to nanoamp leakage values. This prevents damage to sensors or other sensitive signal sources. Second, the MAX358 can withstand a continuous  $\pm 35\text{V}$  overvoltage, imposed by power dissipation considerations.

The digital inputs have logic thresholds of 0.8V and 2.4V, ensuring both TTL and CMOS compatibility without requiring pullup resistors. Break-before-make operation is guaranteed. Power supply currents have been reduced and typical power dissipation is less than 2 milliwatts.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Voltage between Supply Pins	+44V
$V^+$	+22V
$V^-$	-22V
Digital Input Overvoltage:	
$V_{EN}, V_A \{V_{SUPPLY} (+)$	+4V
$\{V_{SUPPLY} (-)$	-4V
Analog Input Overvoltage with Multiplexer On:	
$V_S \{V_{SUPPLY} (+)$	+20V
$\{V_{SUPPLY} (-)$	-20V
Analog Input Overvoltage with Multiplexer Off:	
$V_S \{V_{SUPPLY} (+)$	+35V
$\{V_{SUPPLY} (-)$	-35V
Continuous Current, S or D	20mA
Peak Current, S or D	
(Pulsed at 1ms, 10% duty cycle max)	40mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )	
16-Pin PDIP	842mW
16-Pin WSO	762mW
Derates above +70°C	
16-Pin PDIP	10.5mW/°C
16-Pin WSO	9.5mW/°C

## II. Manufacturing Information

A. Description/Function:	Fault-Protected Analog Multiplexer
B. Process:	M6HV (5 micron metal gate CMOS)
C. Number of Device Transistors:	168
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines or Malaysia
F. Date of Initial Production:	April, 1988

## III. Packaging Information

A. Package Type:	<b>16-Lead PDIP</b>	<b>16-Lead WSO</b>
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0301-0513	# 05-0301-0515
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1

## IV. Die Information

A. Dimensions:	133x160 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Executive Director)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{8.35}{192 \times 4389 \times 1360 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

▲  
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 3.64 \times 10^{-9}$$

$$\lambda = 3.64 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-0857) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The AG28 die type has been found to have all pins able to withstand a transient pulse of  $\pm 300\text{V}$  per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX358xxE**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		1360	3
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	WSO	77	0
			PDIP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

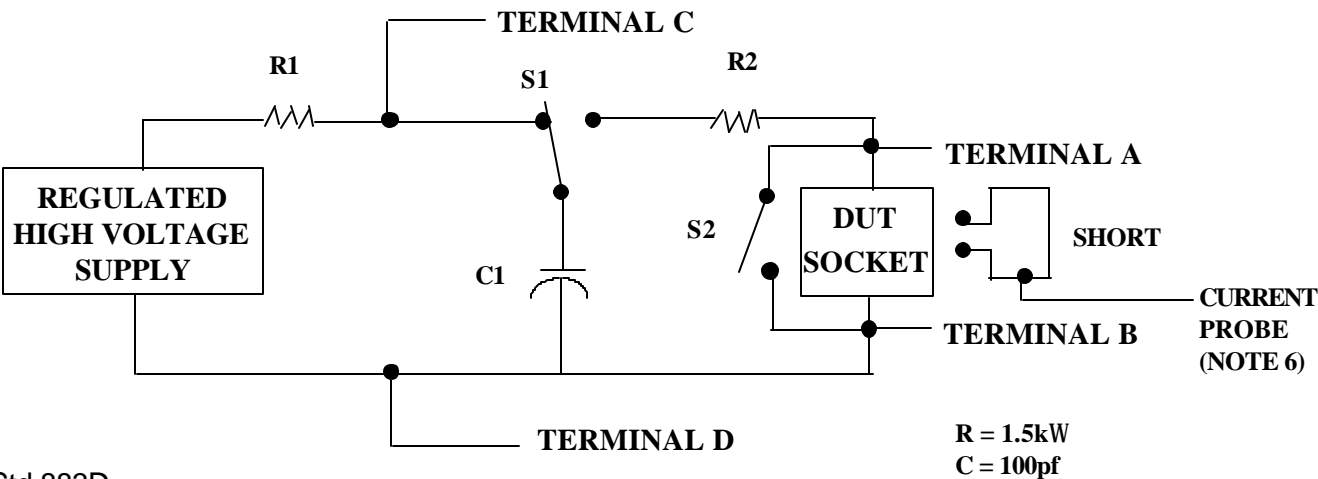
TABLE II. Pin combination to be tested. 1/ 2/

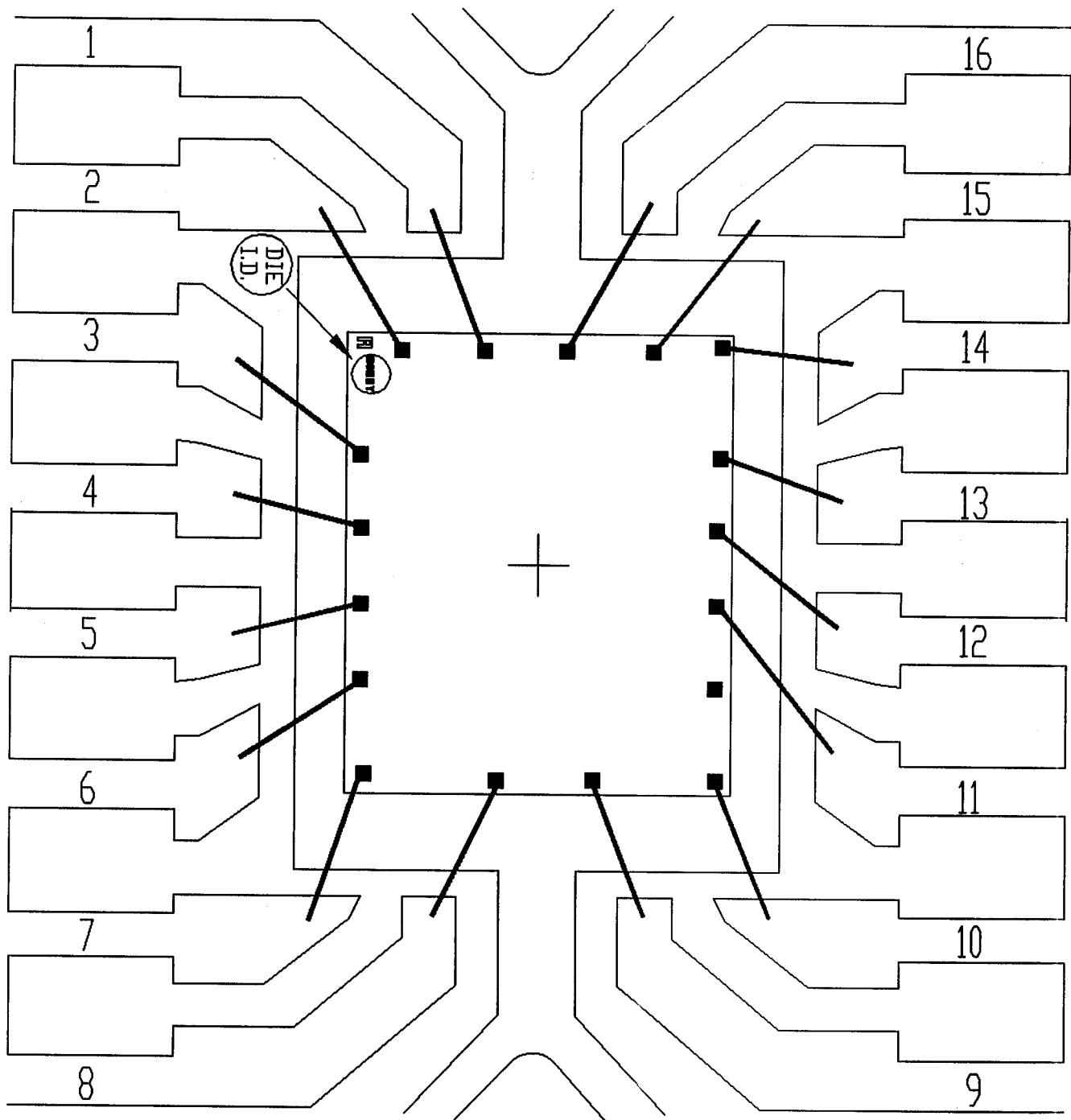
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.  
2/ No connects are not to be tested.  
3/ Repeat pin combination I for each named Power supply and for ground  
(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: W16-3

CAV./PAD SIZE: 160 X 200

APPROVALS

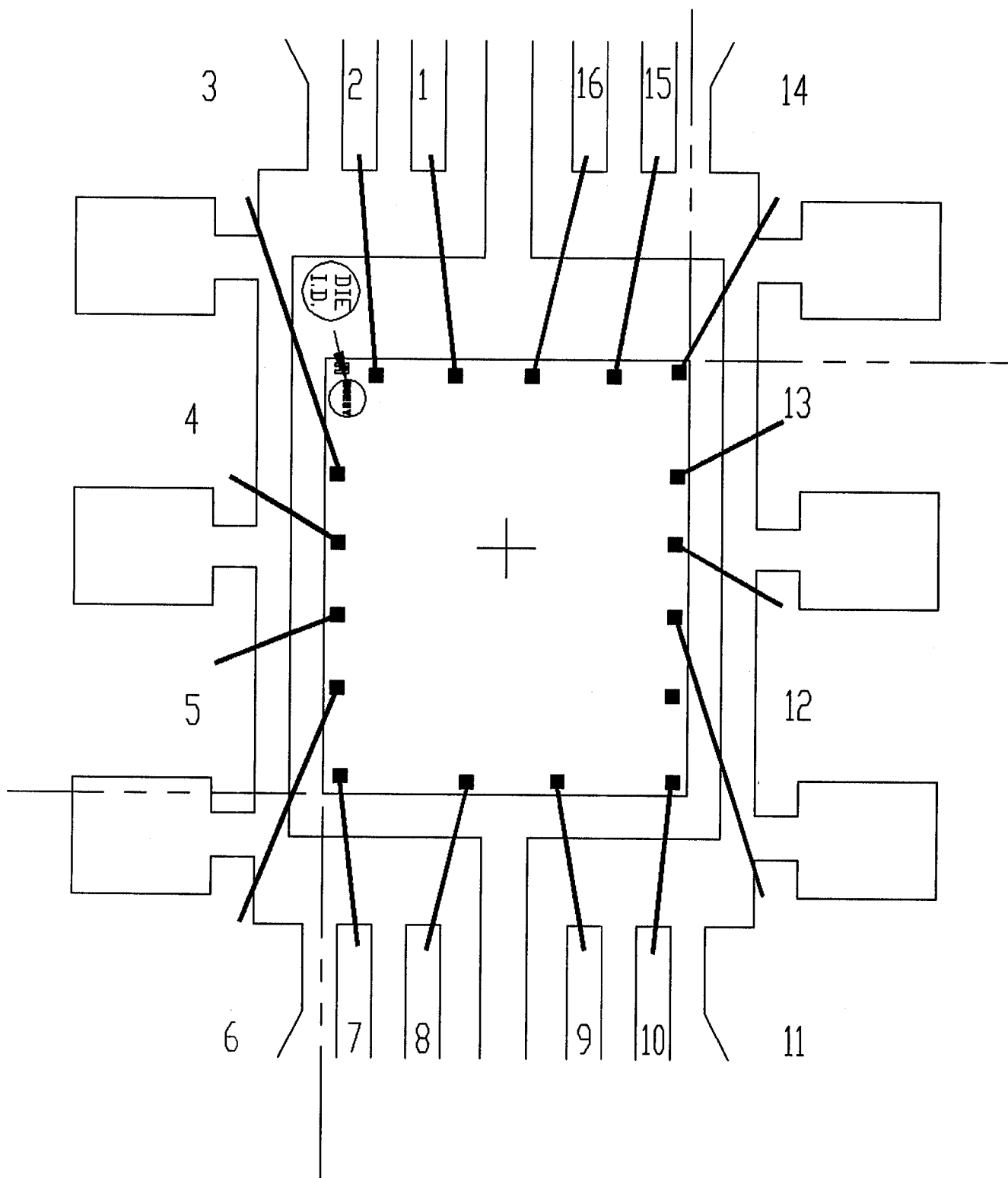
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**MAXIM**

BUILDSHEET NUMBER:  
05-0301-0515

REV.:  
A

PKG.  
DESIGN



PKG.CODE: P16-3

CAV./PAD SIZE:  
150 X 200

APPROVALS

DATE

**MAXIM**

BUILDSHEET NUMBER:  
05-0301-0513

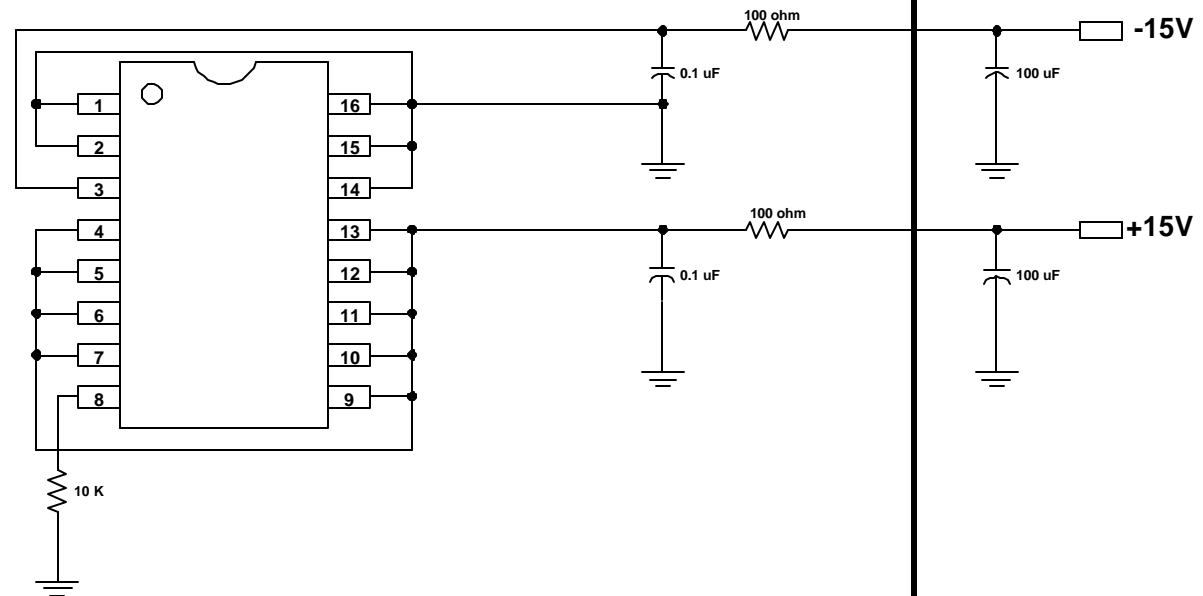
REV.:  
A

PKG.  
DESIGN



# ONCE PER SOCKET

# ONCE PER BOARD



DEVICES: MAX 308/328/338/358/378/354/4708 DG 408/508 IH6108

MAX4508/HI1-0508A-2. PACKAGE: 16-DIP

Max current:(+/-15v) 50uA. For MAX4508/4708 Max current = 350uA.

DRAWN BY: HAK TAN

NOTES: