

RELIABILITY REPORT  
FOR  
MAX354EWE+  
PLASTIC ENCAPSULATED DEVICES

January 22, 2015

**MAXIM INTEGRATED**

160 RIO ROBLES  
SAN JOSE, CA 95134

<b>Approved by</b>
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Quality Assurance
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## Conclusion

The MAX354EWE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX354/MAX355 fault-protected multiplexers (muxes) use a series N-channel, P-channel, N-channel structure that protects the devices from overvoltage up to 40V beyond the supply rails during power-up, power-down, and fault conditions. The MAX354/MAX355 also protect sensitive circuit components against voltages near or beyond the normal supplies. The MAX354 single 8-channel mux and the MAX355 dual 4-channel mux protect analog signals while operating from a single 4.5V to 36V supply or  $\pm 4.5V$  to  $\pm 18V$  dual supplies. These muxes have 350  $\Omega$  on-resistance and can be used for demultiplexing as well as multiplexing. Input leakage current is less than 0.5nA at +25°C and less than 5nA at +85°C. All digital inputs have 0.8V and 2.4V logic thresholds, ensuring both TTL and CMOS logic compatibility without pull-up resistors. Break-before-make operation is guaranteed and power consumption is less than 1.5mW.

**II. Manufacturing Information**

A. Description/Function:	Fault-Protected Analog Multiplexers
B. Process:	S5
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Philippines
F. Date of Initial Production:	Pre 1997

**III. Packaging Information**

A. Package Type:	16-pin SOIC (W)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0301-0696
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	105°C/W
K. Single Layer Theta Jc:	22°C/W
L. Multi Layer Theta Ja:	70°C/W
M. Multi Layer Theta Jc:	23°C/W

**IV. Die Information**

A. Dimensions:	115X130 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- |                                   |   |
|-----------------------------------|---|
| A. Quality Assurance Contacts:    | Don Lipps (Manager, Reliability Engineering)<br>Bryan Preeshl (Vice President of QA)            |
| B. Outgoing Inspection Level:     | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% for all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm  |
| D. Sampling Plan:                 | Mil-Std-105D  |

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 4340 \times 79 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 2.67 \times 10^{-9}$$

$$\lambda = 2.67 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S5 Process results in a FIT Rate of 0.09 @ 25C and 1.53 @ 55C (0.8 eV, 60% UCL).

### B. E.S.D. and Latch-Up Testing (lot NHYAB2039C, D/C 0331)

The AG73 die type has been found to have all pins able to withstand a HBM transient pulse of +/-200V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX354EWE+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	79	0	NHYAB2039C, D/C 0331

Note 1: Life Test Data may represent plastic DIP qualification lots.