RELIABILITY REPORT

FOR

MAX3394EETA+T / MAX3394EEBL+T

PLASTIC ENCAPSULATED / CHIP SCALE DEVICES

April 29, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3394EETA+T / MAX3394EEBL+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3394E/MAX3395E/MAX3396E bidirectional level translators provide level shifting required for data transfer in a multivoltage system. Internal slew-rate enhancement circuitry features 10mA current-sink and 15mA current-source drivers to isolate capacitive loads from lower current drivers. In open-drain systems, slew-rate enhancement enables fast data rates with larger pullup resistors and increased bus load capacitance. Externally applied voltages, VCC and VL, set the logic-high levels for the device. A logic-low signal on one I/O side of the device appears as a logic-low signal on the opposite I/O side, and vice-versa. Each I/O line is pulled up to VCC or VL by an internal pullup resistor, allowing the devices to be driven by either push-pull or open-drain drivers. The MAX3394E/MAX3395E/MAX3396E feature a tri-state output mode, thermal-shutdown protection, and ±15kV Human Body Model (HBM) ESD protection on the VCC side for greater protection in applications that route signals externally. The MAX3394E/MAX3395E/MAX3396E accept VCC voltages from +1.65V to +5.5V, and VL voltages from +1.2V to VCC, making them ideal for data transfer between low voltage ASIC/PLDs and higher voltage systems. The MAX3394E/MAX3395E/MAX3396E operate at a guaranteed data rate of 6Mbps with push-pull drivers and 1Mbps with open-drain drivers. The MAX3394E is a dual-level translator available in 9-bump UCSP(tm) and 8-pin 3mm × 3mm TDFN packages. The MAX3395E is a quad-level translator available in 12-bump UCSP, and 12-pin 4mm x 4mm TQFN packages. The MAX3396E is an octal-level translator available in 20-bump UCSP and 20-pin 5mm × 5mm TQFN packages. The MAX3394E/MAX3395E/MAX3396E operate over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry	
B. Process:	C6	
C. Number of Device Transistors:	882	
D. Fabrication Location:	USA	
E. Assembly Location:	China, Malaysia, Taiwan and Thailand	USA
F. Date of Initial Production:	October 22, 2005	

III. Packaging Information

A. Package Type:	8-pin TDFN	9-pin WLP 3x3 array
B. Lead Frame:	Copper	N/A
C. Lead Finish:	100% matte Tin	N/A
D. Die Attach:	Conductive	None
E. Bondwire:	Au (1 mil dia.)	N/A (N/A mil dia.)
F. Mold Material:	Epoxy with silica filler	None
G. Assembly Diagram:	#05-9000-1919	#05-9000-1918
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	54°C/W	°C/W
K. Single Layer Theta Jc:	8°C/W	°C/W
L. Multi Layer Theta Ja:	41°C/W	211°C/W
M. Multi Layer Theta Jc:	8°C/W	°C/W

IV. Die Information

A. Dimensions:	61 X 61 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1-3 = 0.9 microns (as drawn)
F. Minimum Metal Spacing:	Metal1-3 = 0.9 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the C6 Process results in a FIT Rate of 0.2 @ 25C and 3.4 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The RT94 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 1000V per JEDEC JESD22-A114 (lot S4MABA005A, D/C 0934)
ESD-CDM:	+/- 750V per JEDEC JESD22-C101 (lot S4MABA011C, D/C 0952)

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78 (lot S4MABA005A, D/C 0934).

Table 1
Reliability Evaluation Test Results

MAX3394EETA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	S4MAAQ001C, D/C 0534

Note 1: Life Test Data may represent plastic DIP qualification lots.