

RELIABILITY REPORT

FOR

MAX3392EEUD+ (MAX3372E-MAX3379E and MAX3390E-MAX3393E)

PLASTIC ENCAPSULATED DEVICES

April 9, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by	
Ken Wendel	
Quality Assurance	
Director, Reliability Engineering	



Conclusion

The MAX3392EEUD+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3372E-MAX3379E and MAX3390E-MAX3393E ±15kV ESD-protected level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, VCC and VL, set the logic levels on either side of the device. A low-voltage logic signal present on the VL side of the device appears as a high-voltage logic signal on the VCC side of the device, and vice-versa. The MAX3374E/MAX3375E/MAX3376E/MAX3379E and MAX3390E-MAX3393E unidirectional level translators level shift data in one direction (VL → VCC or VCC → VL) on any single data line. The MAX3372E/MAX3373E and MAX3377E/MAX3378E bidirectional level translators utilize a transmission-gate-based design (Figure 2 in the full data sheet) to allow data translation in either direction (VL ⇔ VCC) on any single data line. The MAX3372E-MAX3379E and MAX3390E-MAX3393E accept VL from +1.2V to +5.5V and VCC from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. All devices in the MAX3372E-MAX3379E, MAX3390E-MAX3393E family feature a three-state output mode that reduces supply current to less than 1μA, thermal shortcircuit protection, and ±15kV ESD protection on the VCC side for greater protection in applications that route signals externally. The MAX3372E/MAX3377E operate at a guaranteed data rate of 230kbps. Slew-rate limiting reduces EMI emissions in all 230kbps devices. The MAX3373E-MAX3376E/MAX3378E/MAX3379E and MAX3390E-MAX3393E operate at a guaranteed data rate of 8Mbps over the entire specified operating voltage range. Within specific voltage domains, higher data rates are possible. (See the Timing Characteristics table in the full data sheet.) The MAX3372E-MAX3376E are dual level shifters available in 3 x 3 UCSP(tm), 8-pin TDFN, and 8-pin SOT23 packages. The MAX3377E/MAX3378E/MAX3379E and MAX3390E-MAX3393E are quad level shifters available in 3 x 4 UCSP, 14-pin TDFN, and 14-pin TSSOP packages.



II. Manufacturing Information

A. Description/Function: ±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level

Translators in UCSP

B. Process: B8

C. Number of Device Transistors:

D. Fabrication Location: Texas

E. Assembly Location: ATP Philippines, UTL Thailand, Carsem Malaysia

F. Date of Initial Production: April 27, 2002

III. Packaging Information

A. Package Type: 14-pin TSSOP
B. Lead Frame: Copper

C. Lead Finish:

D. Die Attach:

Conductive Epoxy

E. Bondwire:

Gold (1 mil dia.)

F. Mold Material:

Epoxy with silica filler

G. Assembly Diagram:

#05-2601-0074

H. Flammability Rating:

Class UL94-V0

I. Classification of Moisture Sensitivity per

JEDEC standard J-STD-020-C

Level 1

J. Single Layer Theta Ja: 110°C/W
K. Single Layer Theta Jc: 30°C/W
L. Multi Layer Theta Ja: 100.4°C/W
M. Multi Layer Theta Jc: 30°C/W

IV. Die Information

A. Dimensions: 80 X 61 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 0.8 microns (as drawn)F. Minimum Metal Spacing: 0.8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.
 H. Isolation Dielectric: SiO₂
 I. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)

Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppmD. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 45 \times 2}$$
 (Chi square value for MTTF upper limit)
(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$x = 23.9 \times 10^{-9}$$

 λ = 23.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the B8 Process results in a FIT Rate of 2.71 @ 25C and 17.30 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The RT40-4 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA.



Table 1

Reliability Evaluation Test Results

MAX3392EEUD+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	
Static Life Test (Note 1)				
,	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0	
Moisture Testing	(Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0	
Mechanical Stress	s (Note 2)				
Temperature	-65°C/150°C	DC Parameters	77	0	
Cycle	1000 Cycles Method 1010	& functionality			

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data